



EXPERT WORKSHOP SERIES

Part 1: Line Differential Protection Basics

Agenda

1 Line Differential Protection Principle

2 Multi-Ended Line Differential Applications

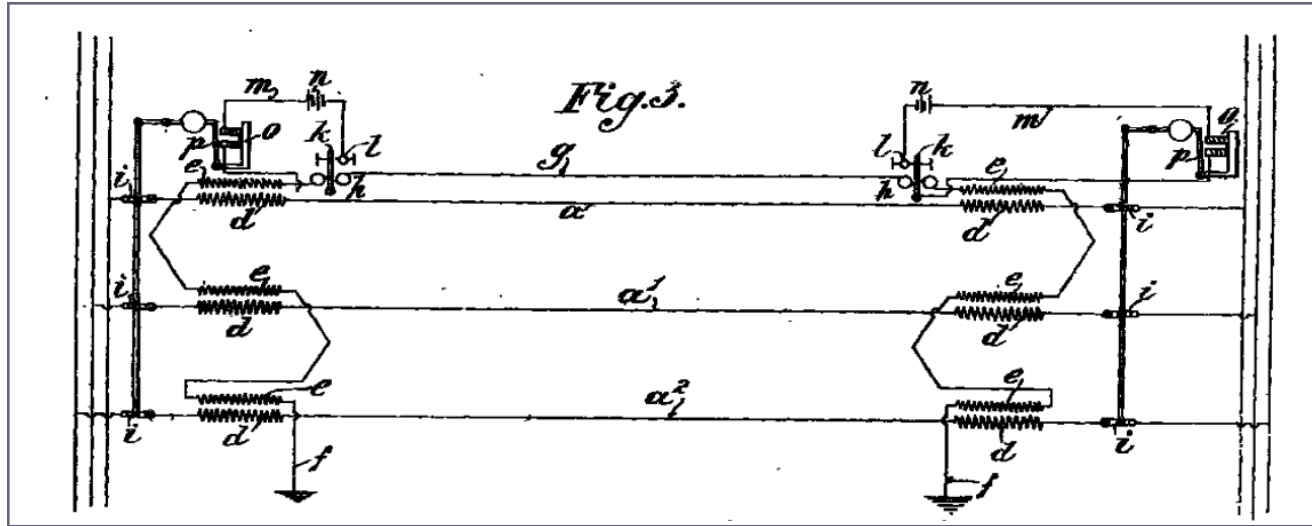
3 SIPROTEC 5 Line Differential Protection

- Data alignment
- Stabilization methods
- Protection stages

Line differential protection principle

History

- 1896 patent DRP92442 (d.c. differential, balanced beams)
- 1899 Schuckert: patent DRP110166 (local line differential)
- 1900 Schuckert: patent DRP113521 (\sim , balanced beams)
- 1904 Merz & Price: patent GB190403896A (pilot wire)



The secondary windings e of the two current transformers are, so relatively arranged that normally the electro-motive forces generated in them balance one another so that no current will flow through the pilot wire g and the relays h , 20

N° 3896



A.D. 1904

Date of Application, 16th Feb., 1904

Complete Specification Left, 13th Oct., 1904—Accepted, 22nd Dec., 1904

PROVISIONAL SPECIFICATION.

Improvements in the Method of and Means for Protecting Apparatus on Alternating Current Systems.

We, CHARLES HESTERMAN MERZ, of 28 Victoria Street in the City of Westminster, Civil Engineer, and BERNARD PRICE, of 34 Holley Avenue, Jesmond, Newcastle-on-Tyne, in the County of Northumberland, Engineer, do hereby declare the nature of this invention to be as follows:—

- 5 In alternating current systems of distribution, it is now usual to transmit electrical energy in the form of alternating current at high pressure from one or more generating stations by feeder cables (hereinafter called feeders) to one or more sub-stations where the energy is reduced to a lower pressure suitable for supply to consumers. In such systems it is usual to provide in connection with each substation, at least two separate feeders and sometimes a larger number of separate feeders to one or more important points on the distributing feeder network, so as to admit of a faulty feeder being cut out without interrupting the supply of energy.

- 10 15 Such a feeder network may, as well understood, be laid out in various ways but the different arrangements usually adopted may be considered as belonging to one or other of the two following systems, or of a combination of them, viz:—
System (a) wherein two feeders extend directly between a generating station and

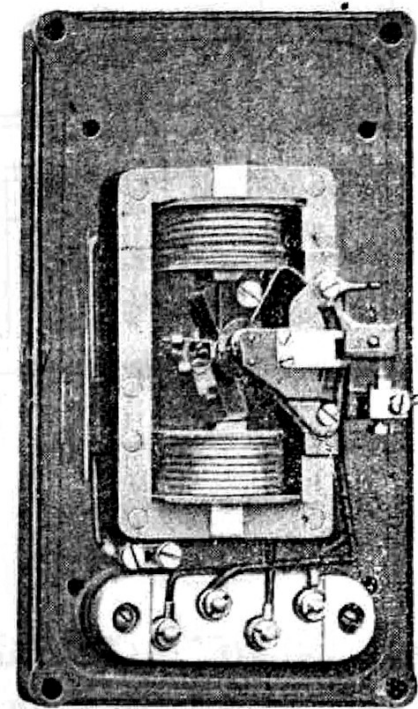
(source: DEPATISnet)

Line differential protection principle

History

Electro - mechanical relays

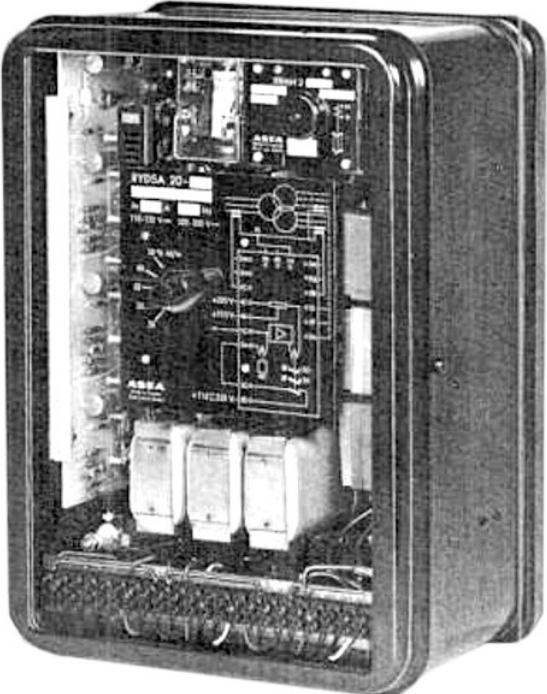
(1910 – 1980)



Sensitive Differential relay, Siemens
(source: W. Schossig, Netzschutzmagazin)

Analog electronic relays

(1960 – 1990)



RYDSA20, ASEA
(source: W. Schossig, Netzschutzmagazin)

Digital processing relays

(1997)



7SD502, Siemens

Line Differential Protection principle

Line Differential Protection Principle

Advantages

- No voltage transformer (VT) needed – only CT's
- 100% of line protected without time delays
- Suitable for:
 - (Short) cables and overhead lines
 - Multi-ended lines (tapped lines)
 - In-zone transformer applications
 - Series compensated lines
- No impact of parallel lines
- No impact of power swings
- All kinds of network grounding
- Sensitive for high resistive and arcing faults
- Simple relay settings

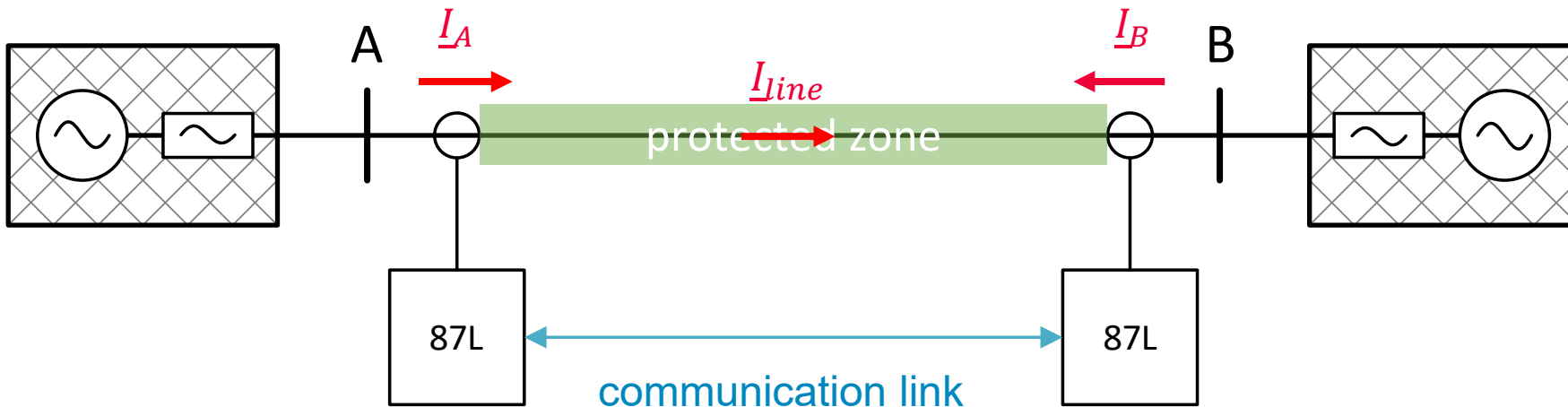
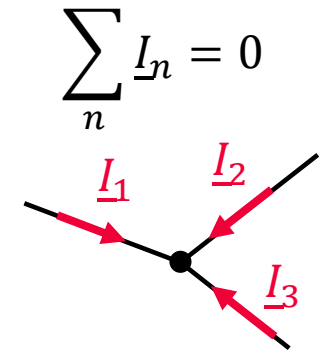
Disadvantages

- Communication channel required
 - Fast
 - Reliable
 - Supervision of communication channel
- No backup protection for external equipment
 - Following lines, transformers, ...
 - Only „in-zone“, defined by CT locations

Line Differential Protection Principle

- Protected zone/object is defined by CT locations → „selectivity“
- Comparison of local phase current and remote end(s) phase current
- Fundamental frequency current phasors (Fourier filters)
- Current measurement towards protected object (line, transformer, ...)
- No operation delay needed → „instantaneous“
- Communication link required between line end(s)

1st Kirchhoff's current law:

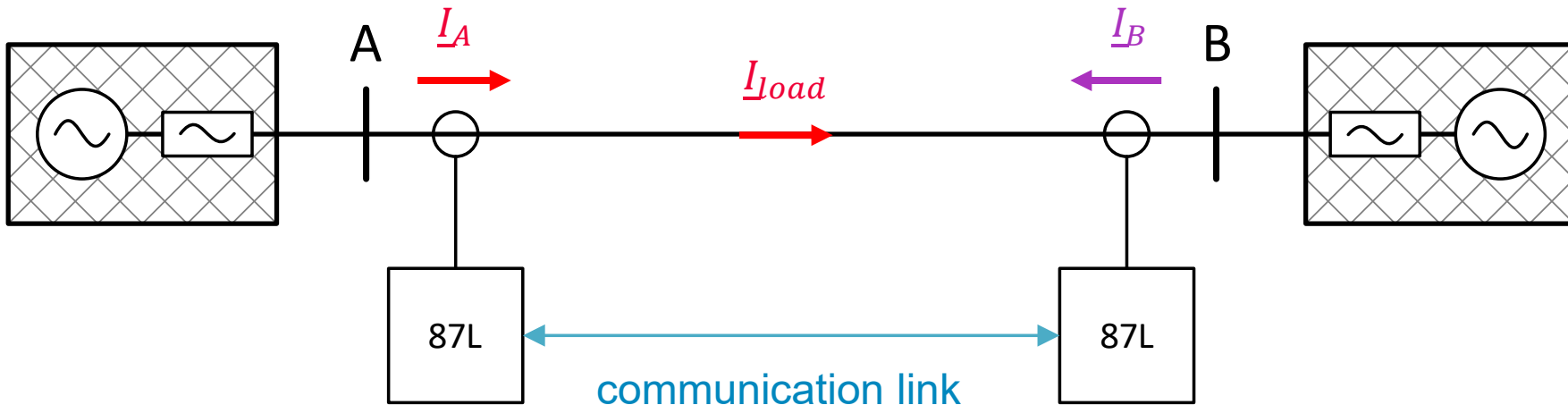
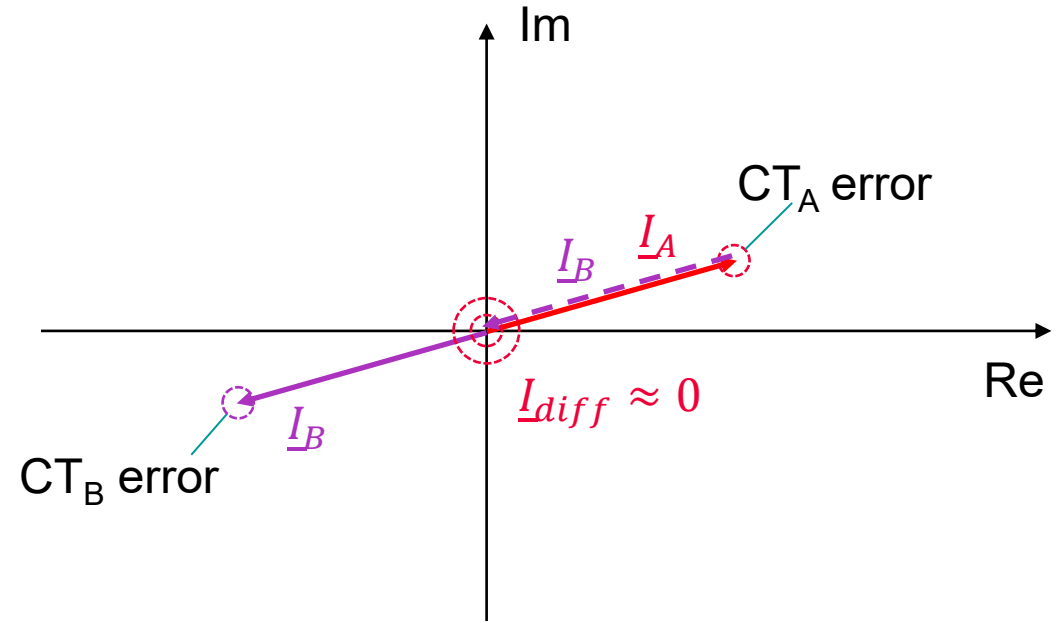


Line Differential Protection Principle

- Normal load condition
 - Small CT errors (phase, amplitude)
 - Small differential current

$$\left| \sum_n \underline{I}_n \right| = I_{diff}$$

$$I_{diff} = |\underline{I}_A + \underline{I}_B|$$

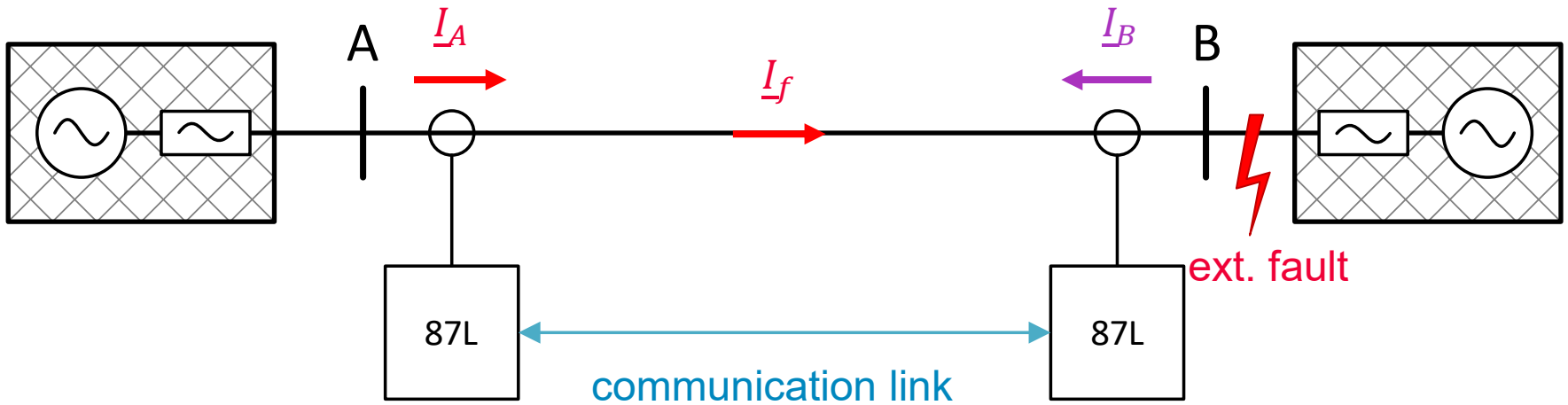
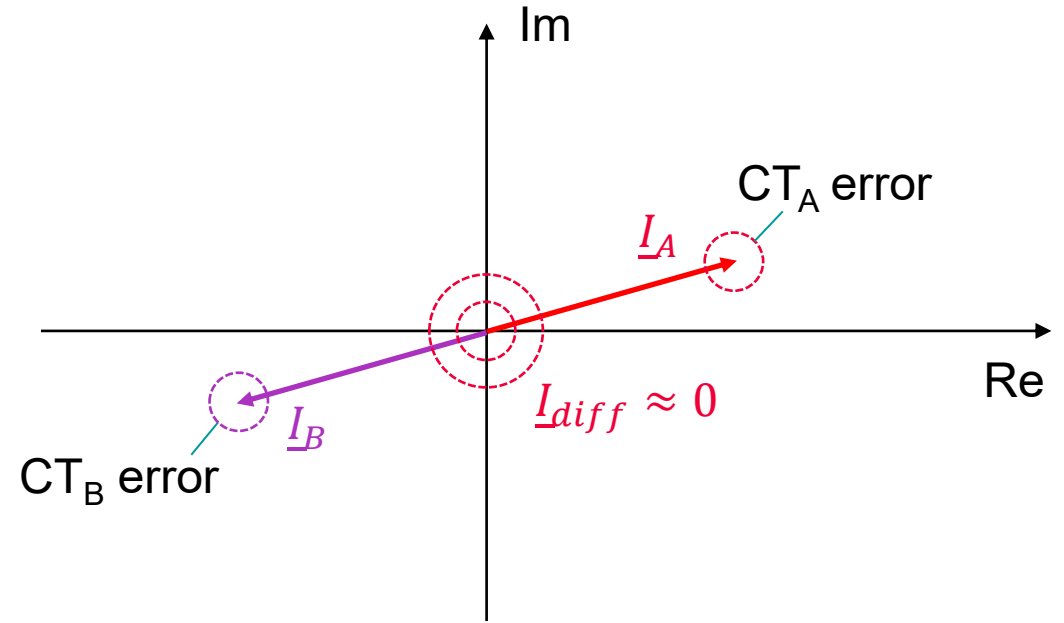


Line Differential Protection Principle

- External fault condition
 - Differential current due to CT errors to consider (phase, amplitude)
 - CT saturation ?
 - Stabilization needed

$$\left| \sum_n \underline{I}_n \right| = I_{diff}$$

$$I_{diff} = |\underline{I}_A + \underline{I}_B|$$

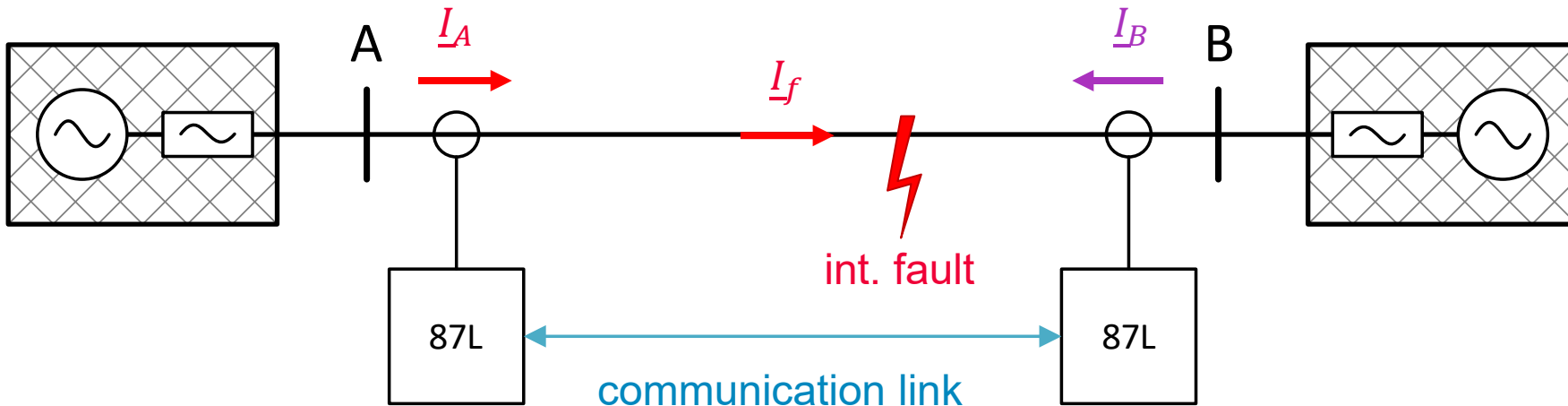
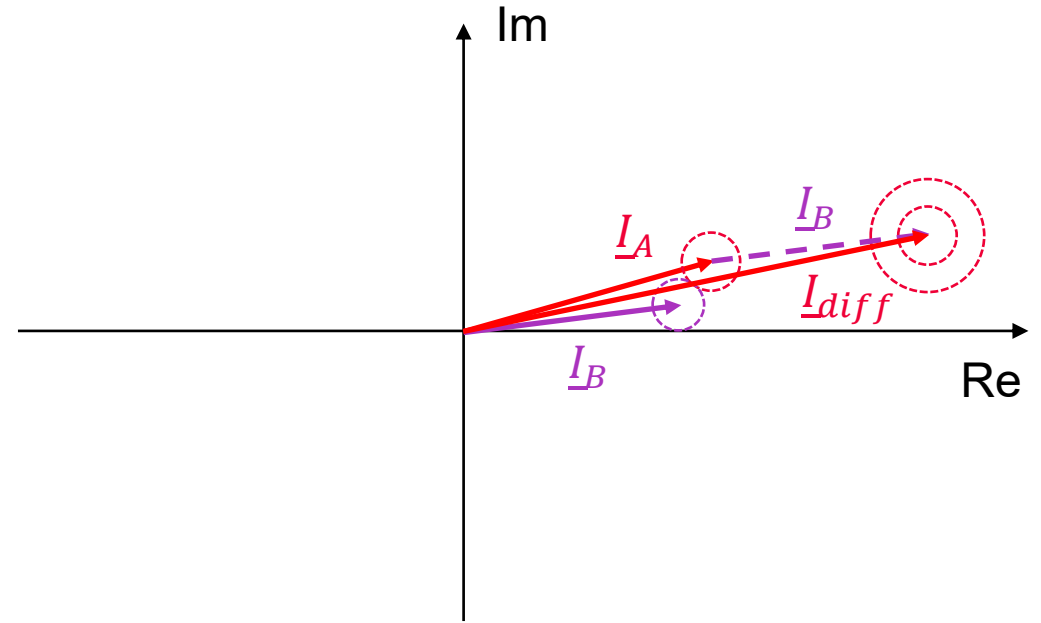


Line Differential Protection Principle

- Internal fault condition
 - High differential current
 - Operate / Trip required

$$\left| \sum_n \underline{I}_n \right| = I_{diff}$$

$$I_{diff} = |\underline{I}_A + \underline{I}_B|$$

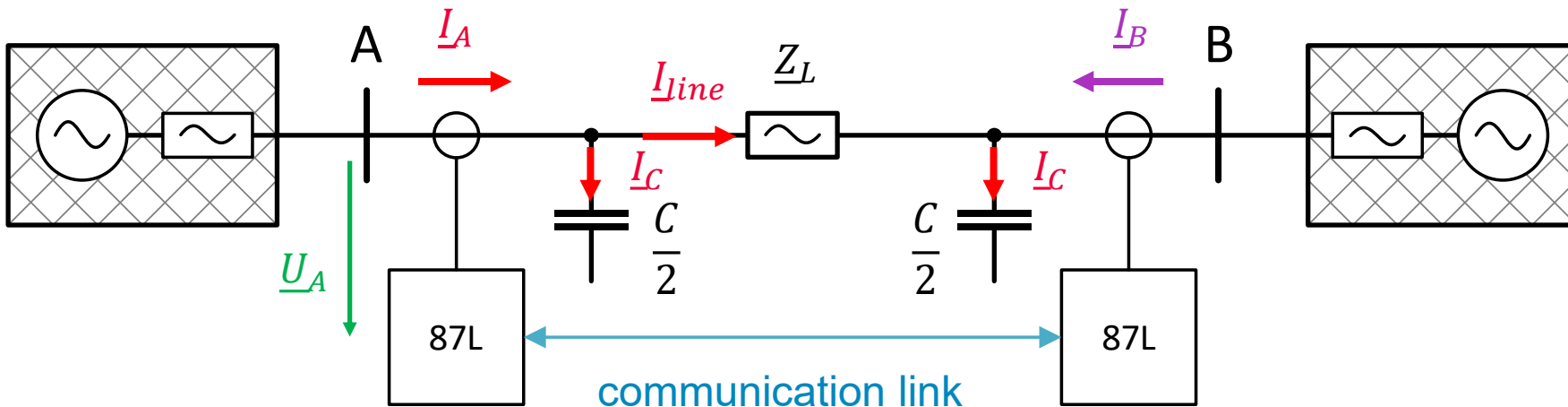
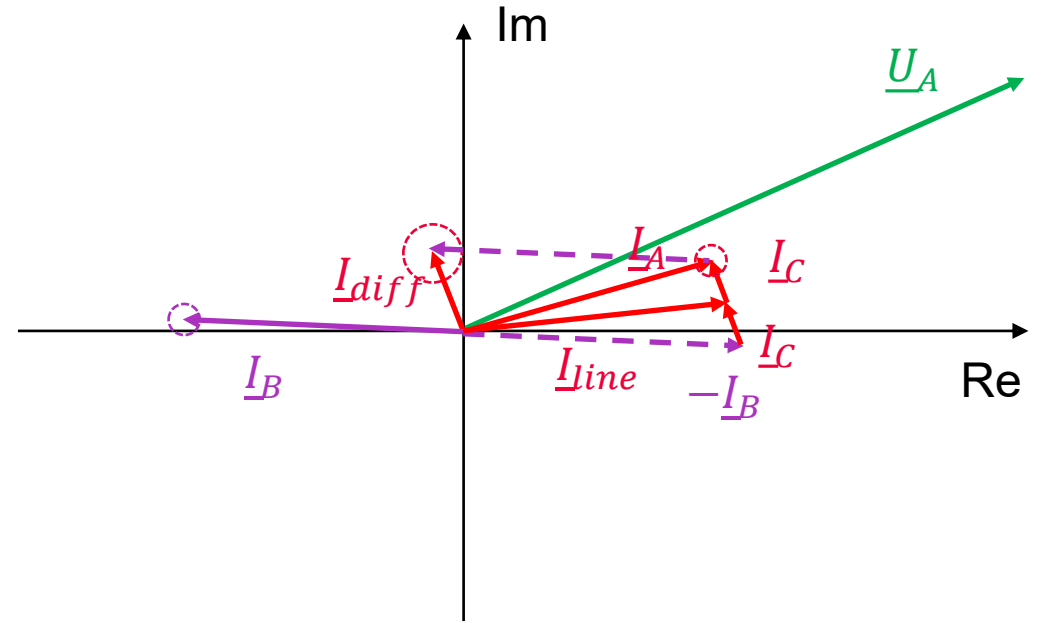


Line Differential Protection Principle

- Capacitive charging current
- Differential current equals line charging current
- Stabilization required

$$\left| \sum_n \underline{I}_n \right| = I_{diff}$$

$$I_{diff} = |\underline{I}_A + \underline{I}_B| = \sum I_C$$



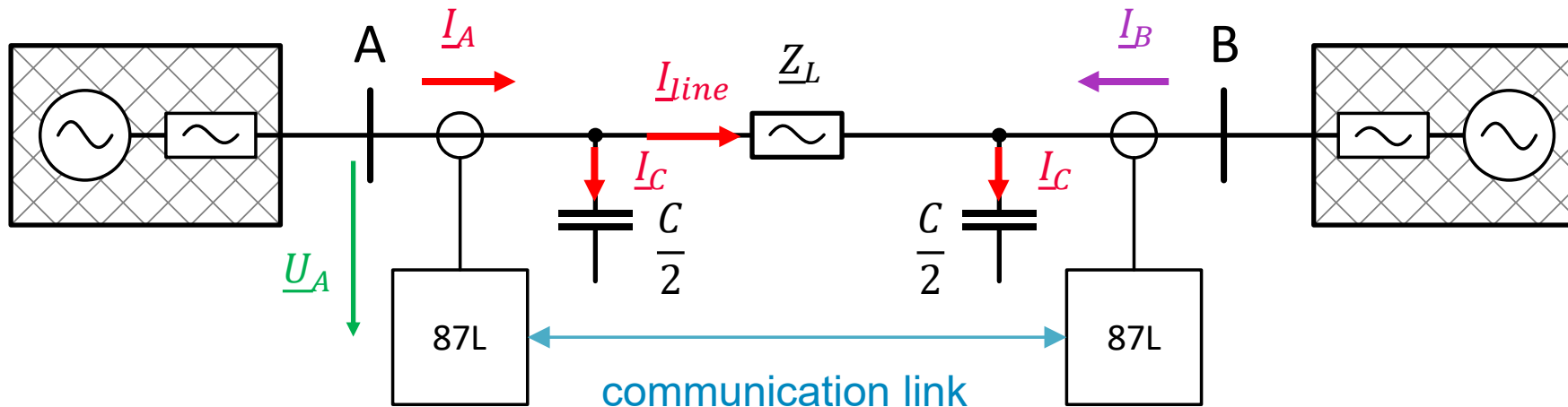
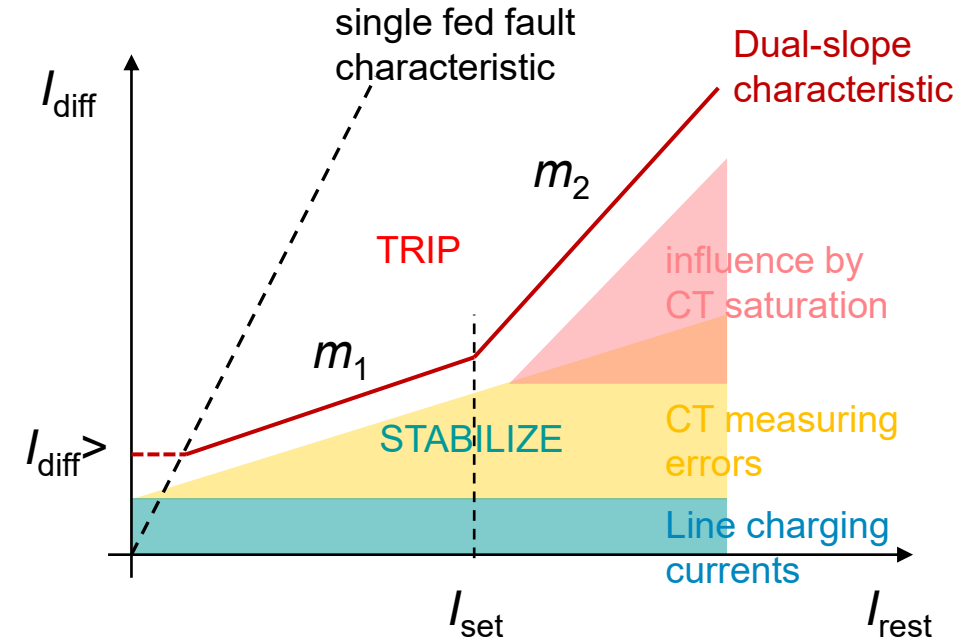
Line differential protection principle

Conventional dual-slope differential characteristic

- Dual-slope characteristic
 - m1 – covers measuring errors
 - m2 – covers also signal distortion (low CT saturation)
 - Factor K depends on vendor
 - Changeover setting: I_{set}

$$I_{diff} = |\underline{I}_A + \underline{I}_B|$$

$$I_{rest} = K \cdot (|\underline{I}_A| + |\underline{I}_B|)$$



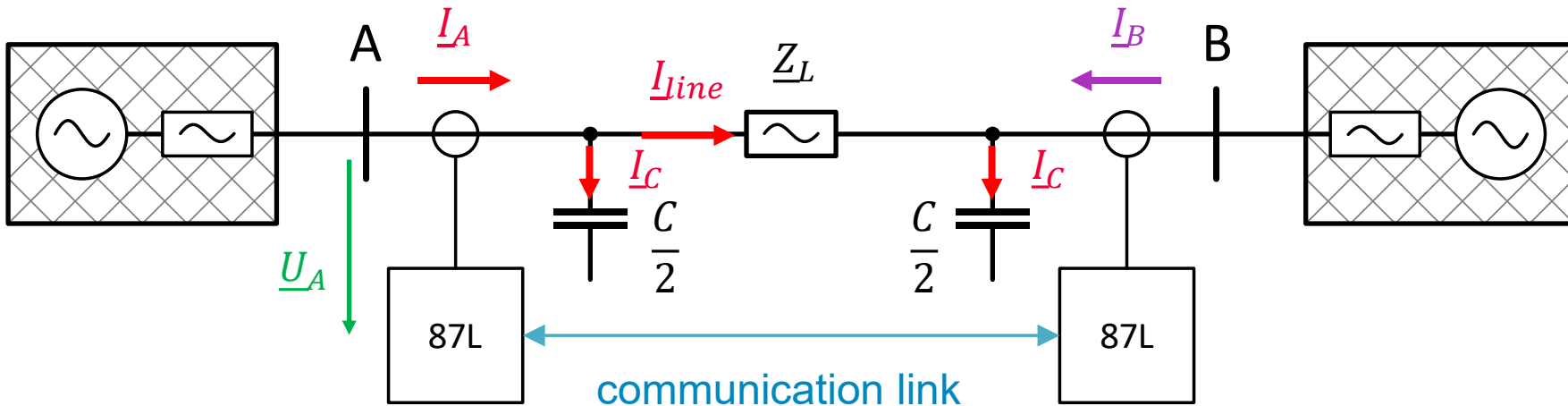
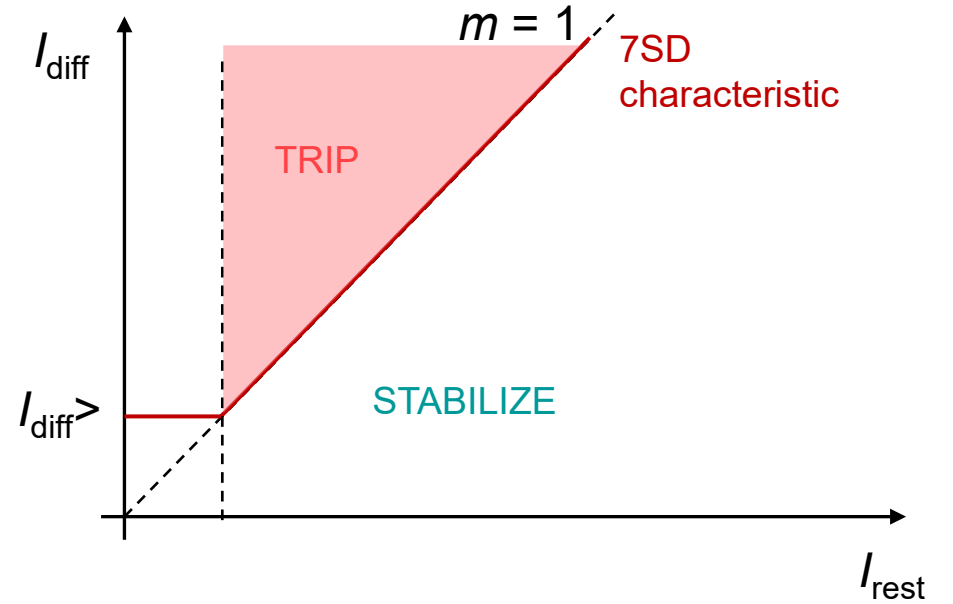
Line differential protection principle

Adaptive restrained differential characteristic – 7SD5/6/8

- Single slope characteristic
 - Fixed 45° slope
 - Adaptive restraining current (incl. measuring errors, signal distortion)

$$I_{diff,ph} = |I_{A,ph} + I_{B,ph}|$$

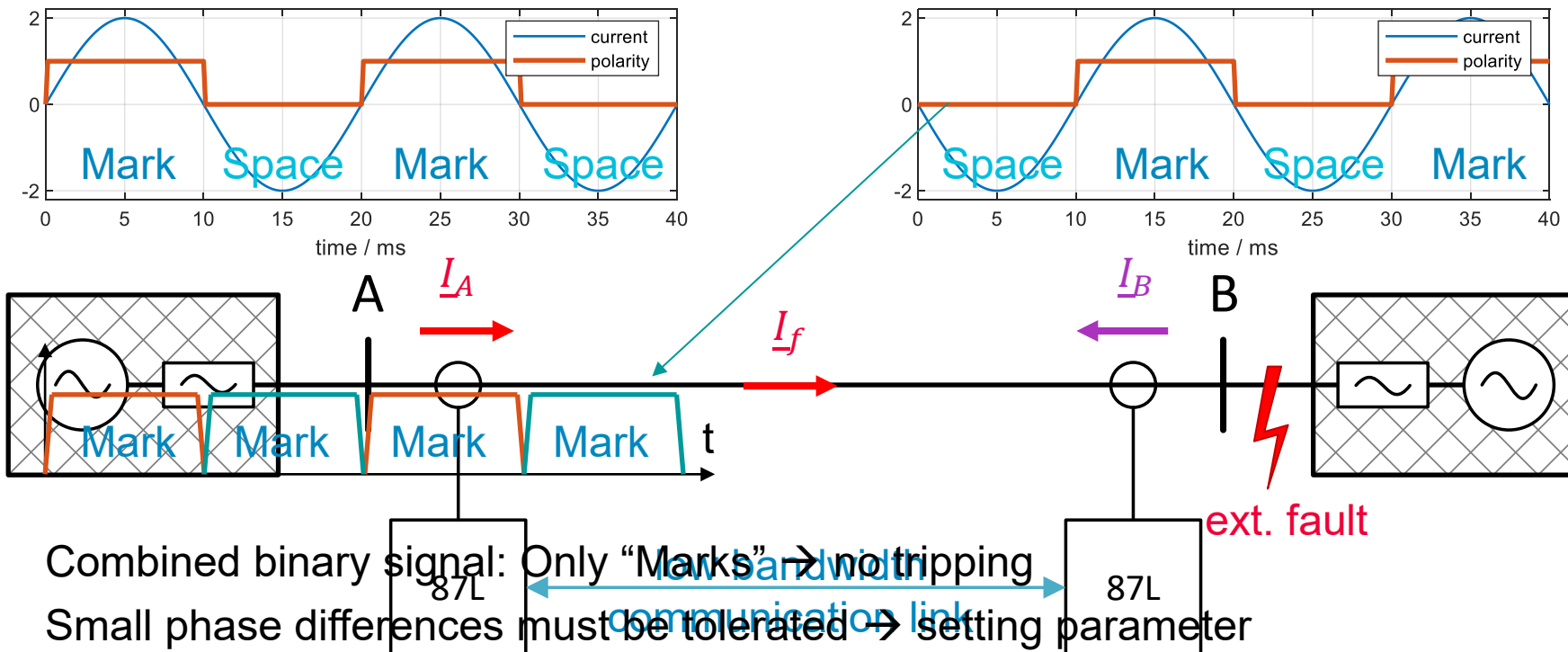
$$I_{rest,ph} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$



Line differential protection principle

Phase comparison principle – 7SD80

- Only exchange of currents polarity (positive sign of fundamental current component)
 - Lower Bandwidth requirements → powerline communication (PLC) sufficient
 - Current amplitude information gets lost (only used for min. current release) → Less accuracy

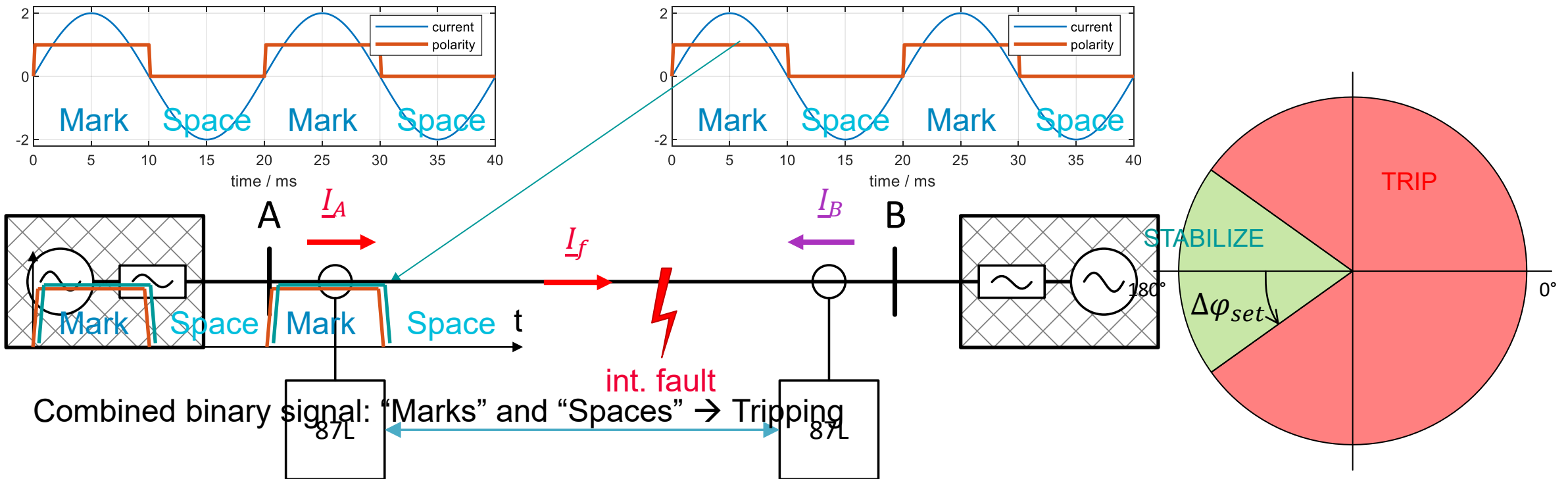


Legacy technology:
 Information "compression"
 3ph currents → one current signal (e.g. neg. sequence current I_2)

Line differential protection principle

Phase comparison principle – 7SD80

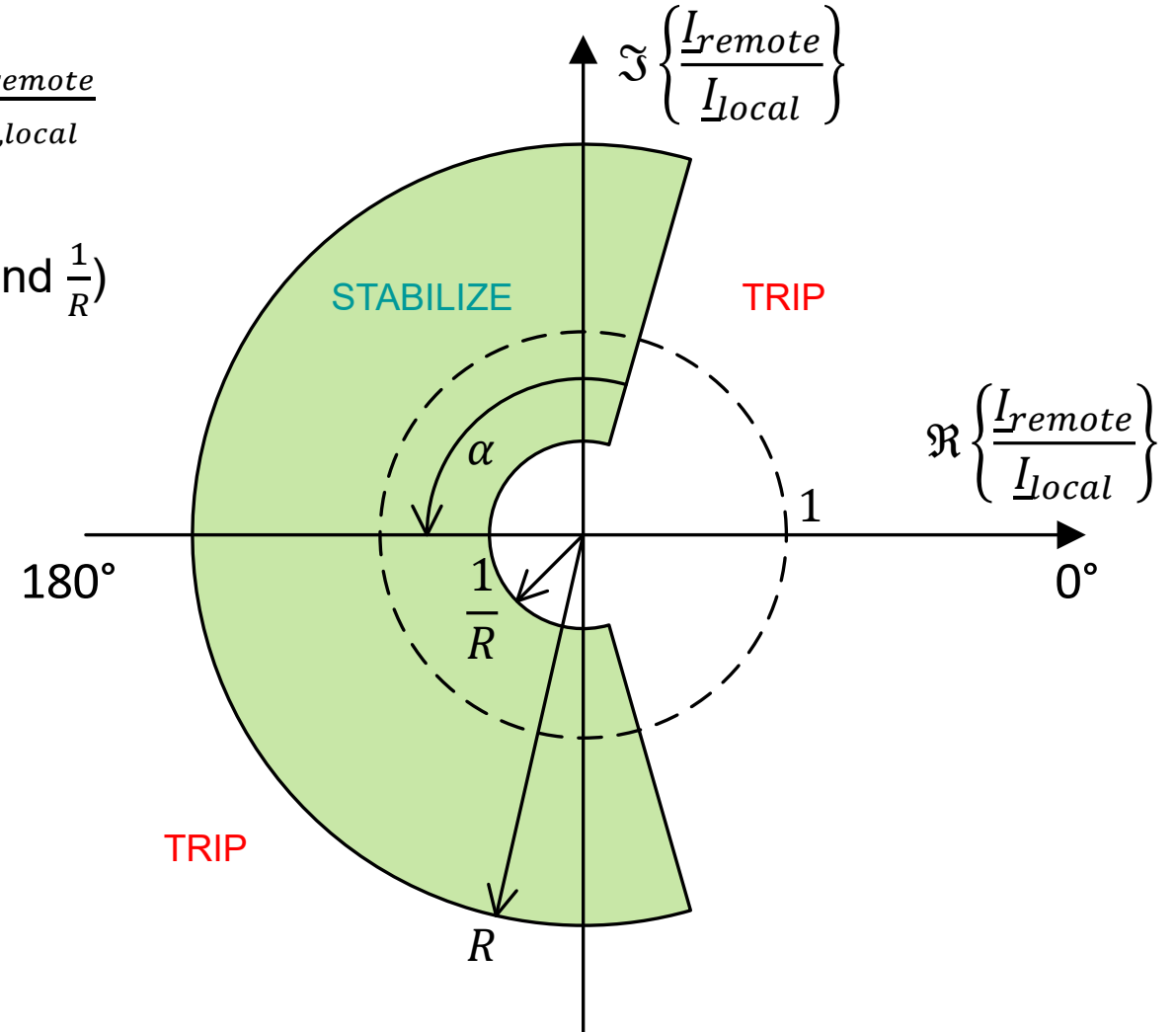
- Only exchange of currents polarity (positive sign of fundamental current component)
 - Lower Bandwidth requirements → powerline communication (PLC) sufficient
 - Current amplitude information gets lost (only used for min. current release) → Less accuracy



Line differential protection principle

Alpha plane characteristic

- Evaluation of the current ratio $\frac{I_{ph,remote}}{I_{ph,local}}$ or $\frac{I_{2,remote}}{I_{2,local}}$ or $\frac{I_{0,remote}}{I_{0,local}}$
 - Principle is similar to phase comparison
 - Considering also current amplitudes (ratio limits: R and $\frac{1}{R}$)
 - Fundamental current component (DFT) calculation
- Stabilization required for
 - External faults with CT saturation

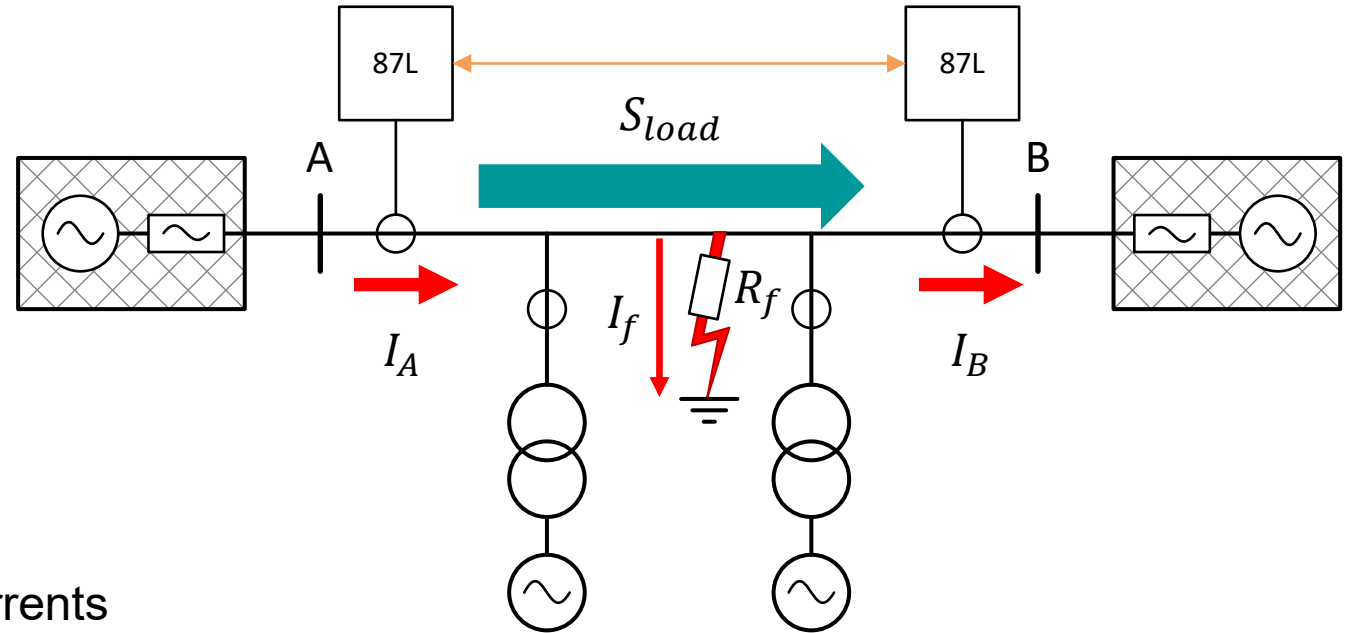


Multi-Ended Line Differential Applications

Multi Ended Line Differential Applications

Tapped Line Application

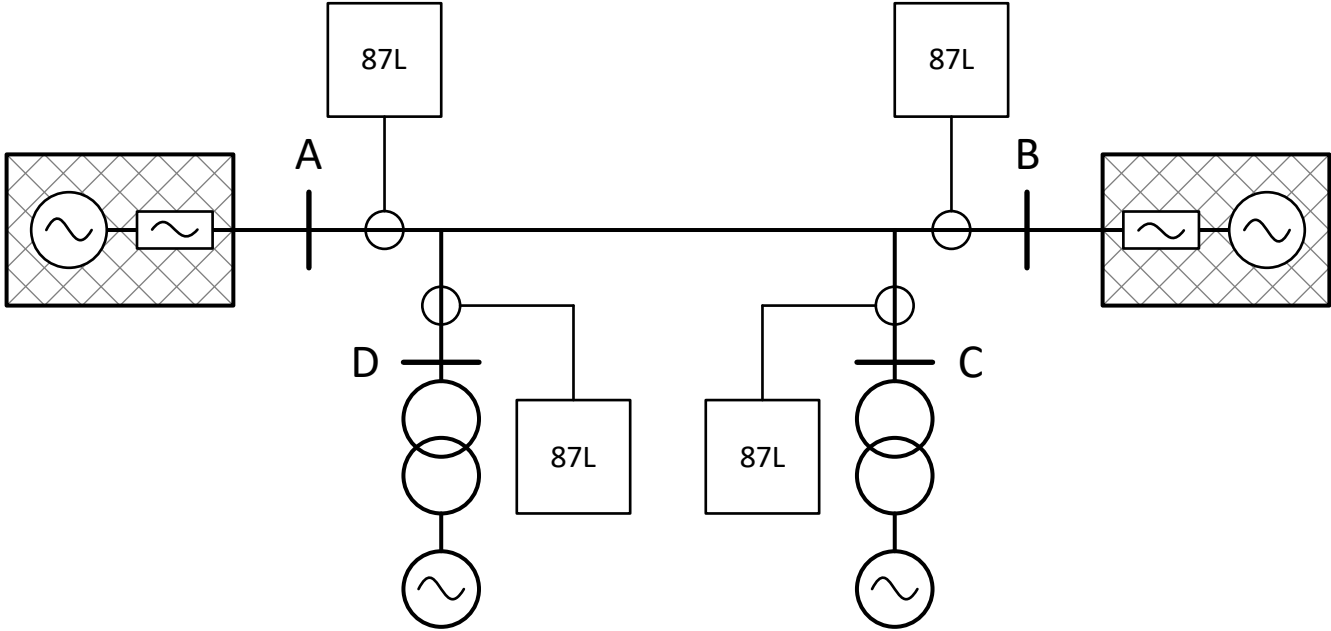
- DER connected to existing lines
 - Smaller generation (wind, PV)
- Smaller / rural load centers
- Differential current setting above infeed
 - Reduced sensitivity for fault currents
- High load current at line → high restraining currents
 - Reduced sensitivity for high impedance faults



Multi Ended Line Differential Applications

Tapped Line Application

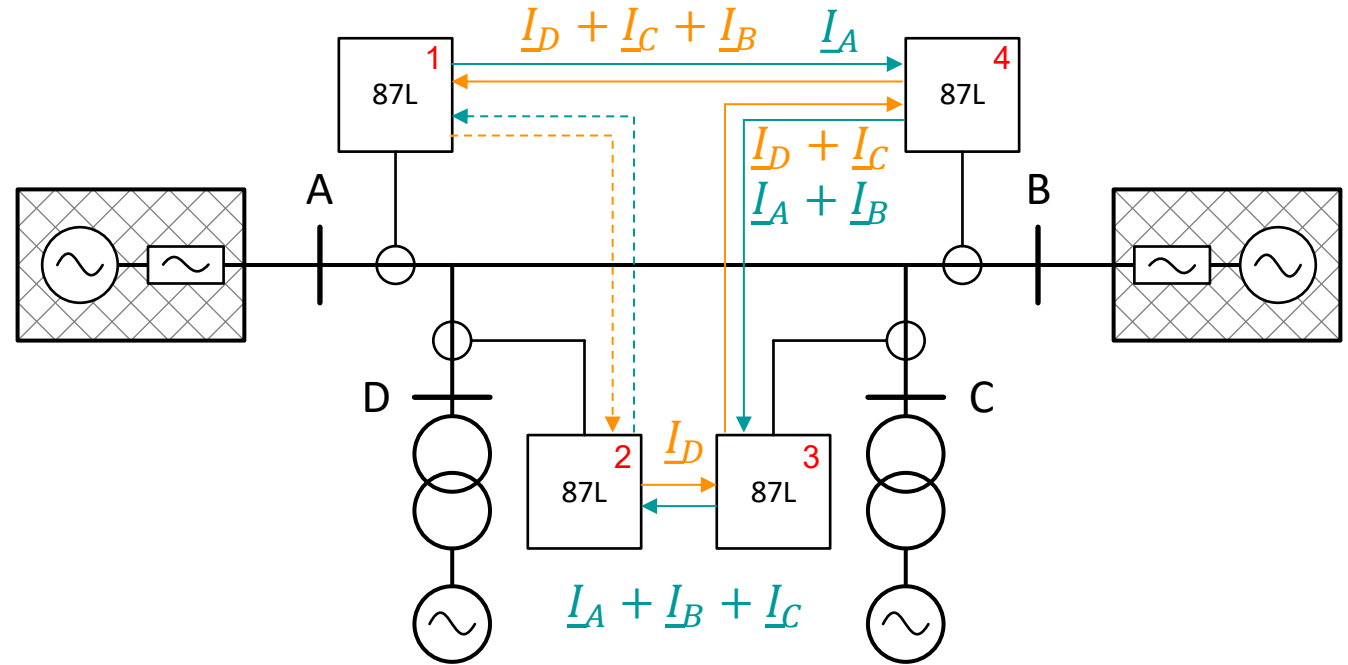
- Larger DER connected to existing lines
- Higher load centers
- Multi-ended line differential protection
 - Communication required to all line ends



Multi Ended Line Differential Applications

Chain or Ring Topology

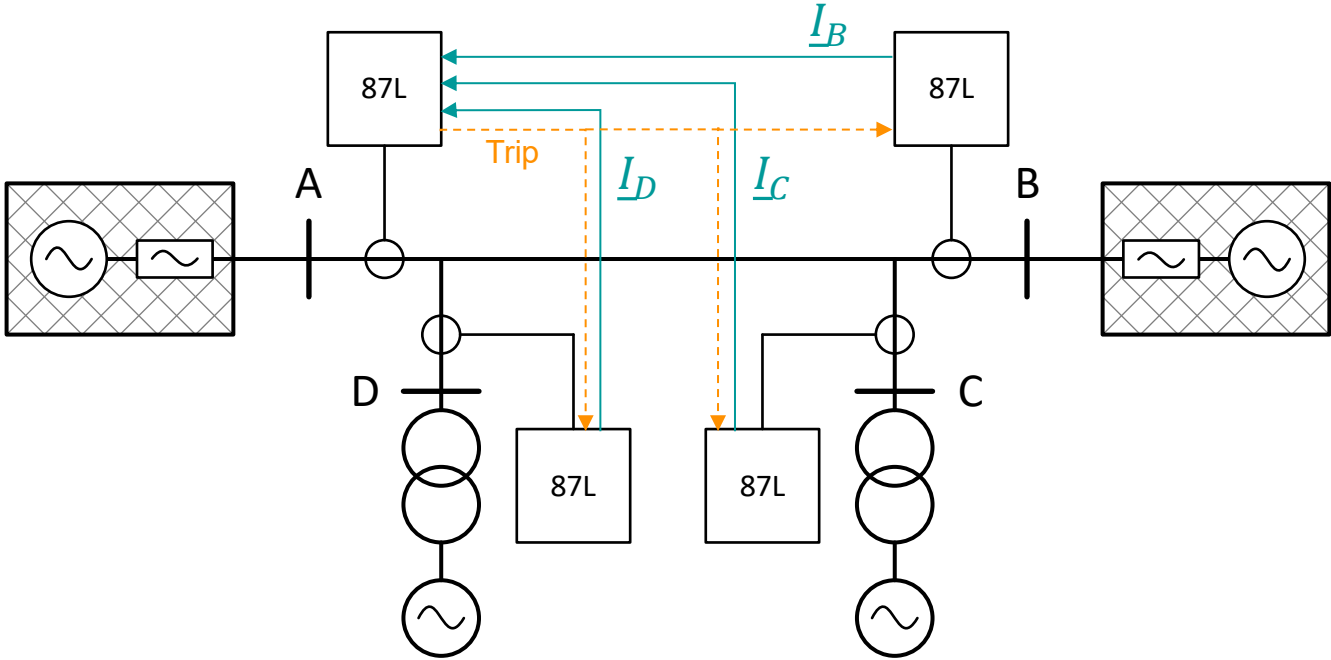
- Chain or Ring topology
 - Standby path in Ring \rightarrow Chain
 - Transmission of partial vector sums
- Applied for SIPROTEC 7SD8



Multi Ended Line Differential Applications

Star Topology

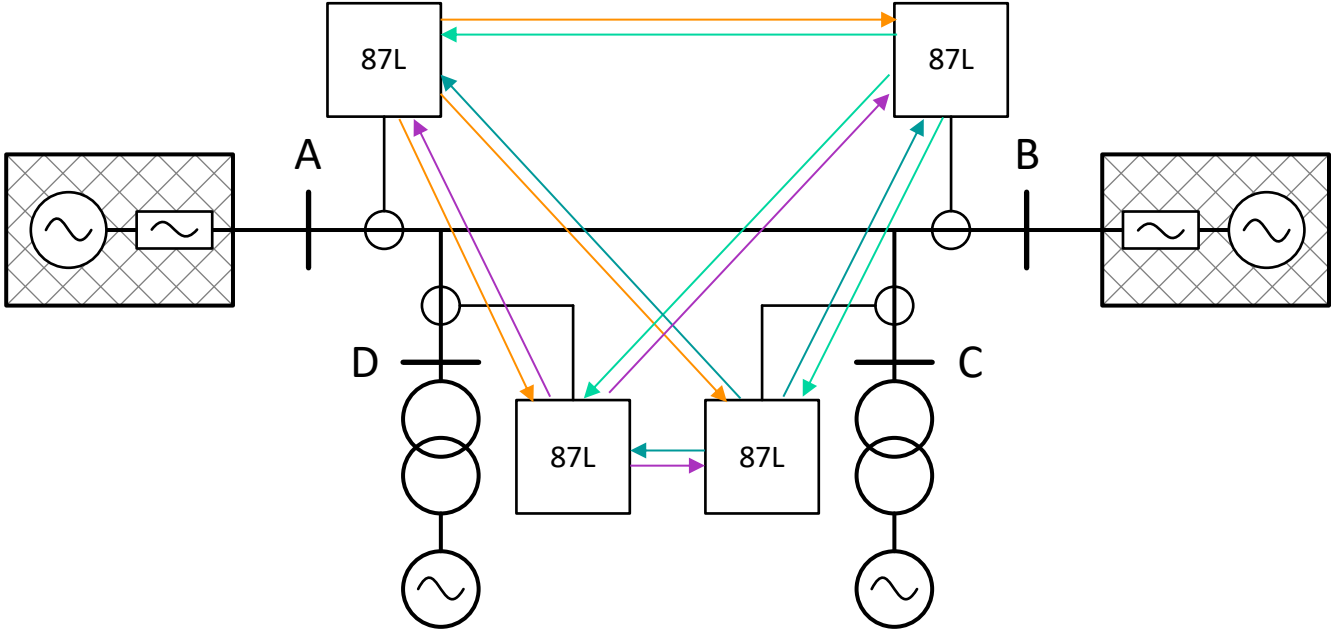
- Star topology
 - Centralized protection (Master-Slave)
 - Decentralized (Master-Master)



Multi Ended Line Differential Applications

Star Topology

- Star topology
 - Centralized protection (Master-Slave)
 - Decentralized (Master-Master)



SIPROTEC 5

Line Differential Protection

Line differential protection

Overview – SIPROTEC series

Hardware,
I/O, Modules



Functionality,
Applications

Line differential protection

Overview – SIPROTEC series

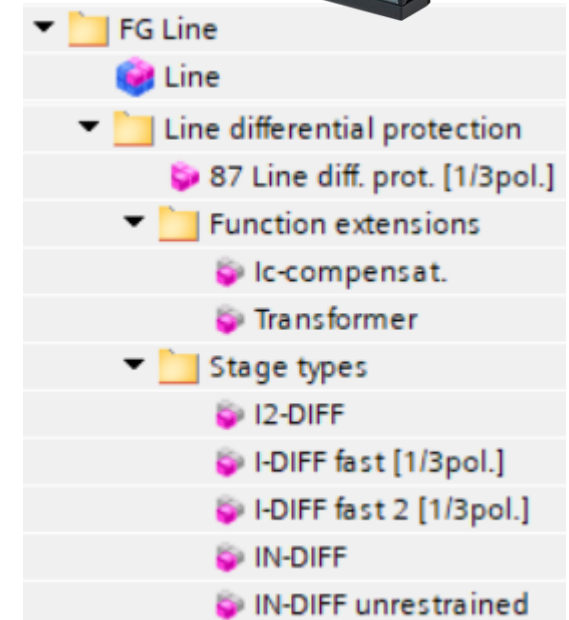
Feature Set	SIPROTEC 4		SIP 4 Compact	SIPROTEC 5					
	7SD61	7SD52	7SD80	7SD82	7SD86	7SD87	7SL82	7SL86	7SL87
Number of line ends	2	2 ... 6	2	2 ... 6	2 ... 6	2 ... 6	2 ... 6	2 ... 6	2 ... 6
Tripping mode, min. T.-time	3-pol., 19ms	1/3-pol., 9ms	3-pol., 21ms	3-pol., 19ms	3-pol., 9ms	1/3-pol., 9ms	3-pol., 19ms	3-pol., 9ms	1/3-pol., 9ms
Transformer on line	●	●	–	●	●	●	●	●	●
Comm.: direct FO (max. km)	100 ¹⁾	100 ¹⁾	24	100 ¹⁾	100 ¹⁾	100 ¹⁾	100 ¹⁾	100 ¹⁾	100 ¹⁾
Comm.: 2-wire Cu (max. km)	20 ²⁾	20 ²⁾	20 (internal)	20 ²⁾	20 ²⁾	20 ²⁾	20 ²⁾	20 ²⁾	20 ²⁾
Comm.: IEEE C37.94	●	●	–	●	●	●	●	●	●
Comm.: G703(1/6), X.21 ²⁾	●	●	–	●	●	●	●	●	●
Comm.: Diff over IP/Eth.	–	–	–	–	●	●	–	●	●
Inputs and Outputs (max. standard variant)	4I, 4U 7BI, 5BO	4I, 4U 24BI, 31BO	4I, 3U 7BI, 9BO	4I, 4U 11BI, 23BO 9BI, 16BO	8I, 8U ¹⁾ 31BI, 46BO ¹⁾	8I, 8U ¹⁾ 31BI, 46BO ¹⁾	4I, 4U 11BI, 23BO 9BI, 16BO	8I, 8U ¹⁾ 31BI, 46BO ¹⁾	8I, 8U ¹⁾ 31BI, 46BO ¹⁾
Distance protection (2 in 1)	–	●	–	–	–	–	●	●	●
SIP 4 Compatibility	NA	NA	–	●	●	●	●	●	●

1) Changeable (modular)

2) Using external communication converter

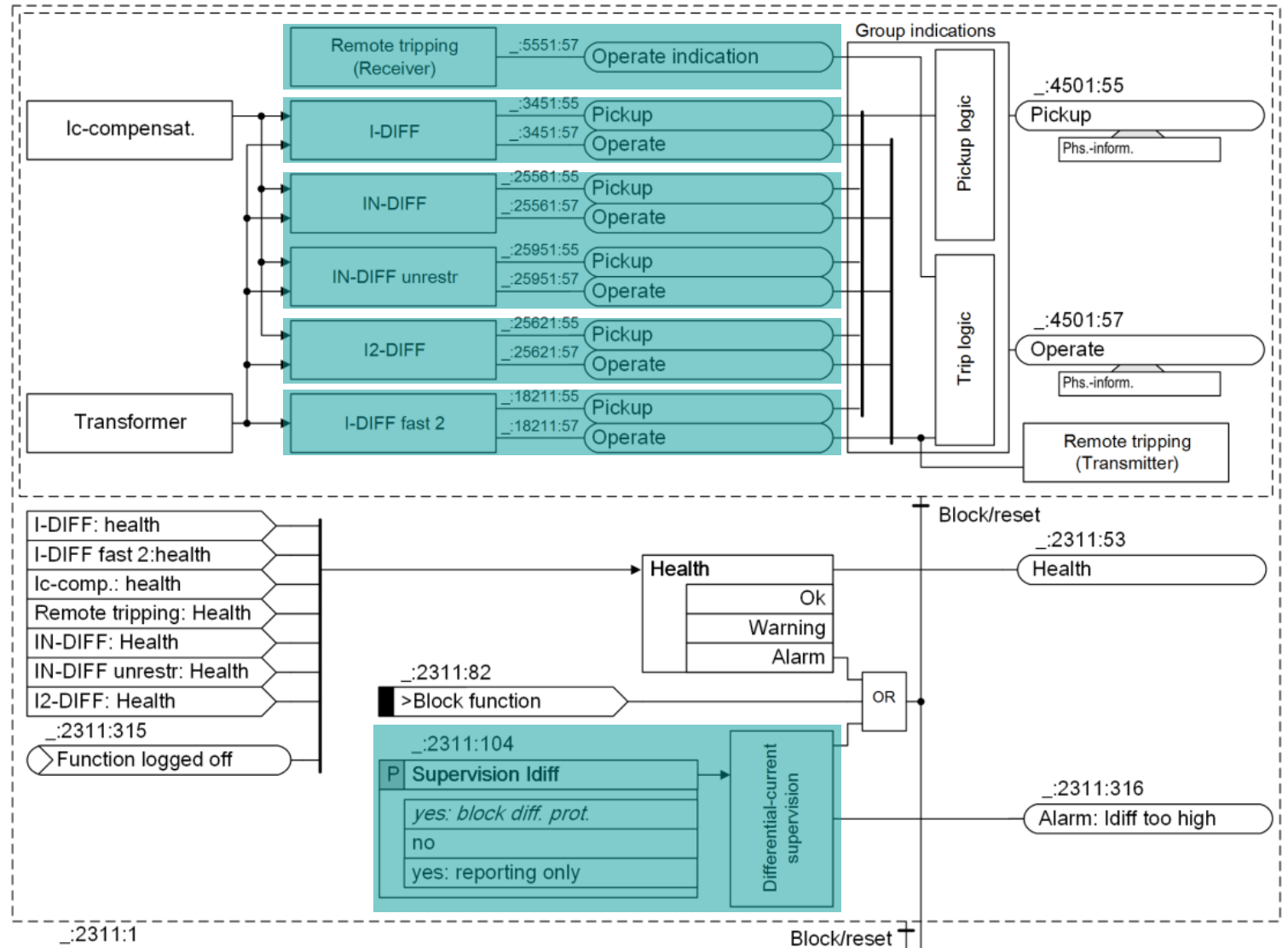
7SD8 Line Differential Protection Overview

- Up to 6 line ends (applications with multiple tapped lines)
 - Transformer in zone protection
 - Capacitive charging current compensation
 - Remote tripping
-
- Several Protection communication interface options
 - Direct fiber connections (long distance)
 - Access to multiplexers (electrical and optical interfaces)
 - Line Differential over IP/Ethernet
 - Line differential test features
 - Local / Loopback / Characteristic
 - Sampled values (SAMU/MU) / test flags



7SD8 Line Differential Protection Overall Logic Diagram

- Core protection stages
 - I-DIFF: sensitive phase current differential
 - I-DIFF fast 2: faster phase current/charge differential
- Additional stages
 - IN-DIFF: sensitive earth differential
 - I2-DIFF: sensitive negative sequence differential
- Features
 - In-zone Transformer protection
 - Charging current compensation
 - Remote tripping (Rx, Tx)
 - Supervision functions



7SD8 Line Differential Protection

General

- Current phasors are estimated from sampled current waveform using FIR filters
- Sample time and data window must not be equal at all line ends → asynchronous phasors
- Alignment of current phasors → current phasor correction → needed for Kirchhoff's law

- For each protection interface:
 - Measure the round trip delay between relays
 - Estimation of DTO (device time offset) → supervise trend of CPU crystal drift
 - Transient compensation of unsymmetrical transmission delays (Tx, Rx channel)

- Line differential protection uses data from synchronized protection interface (with highest bandwidth)

SIPROTEC 5

Line Differential Protection

Data Alignment

7SD8 Line Differential Protection

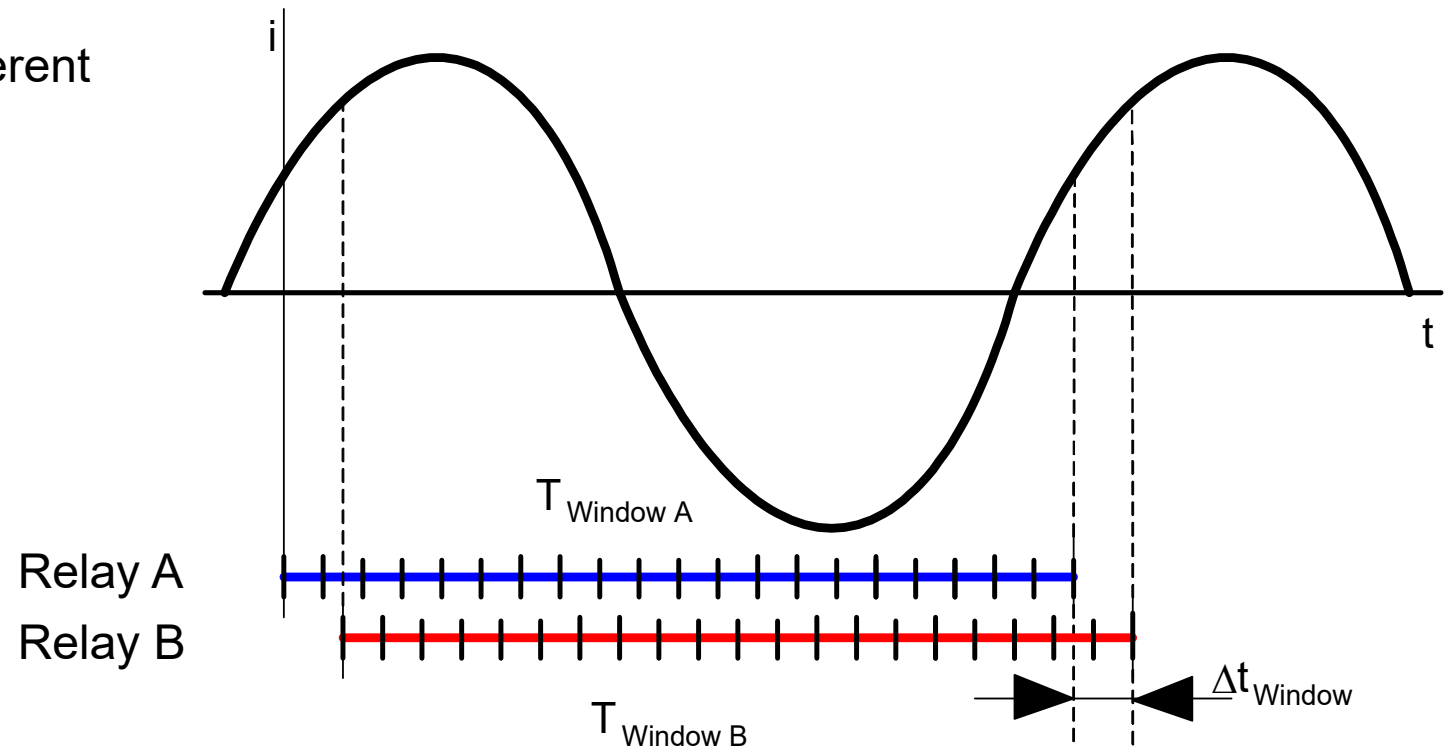
General – Data Alignment

- Timebase counters running independent in both relays (derived from CPU crystal)
- Data windows for phasor calculation is different
- Offset in device times $\rightarrow \Delta t_{Window}$

\rightarrow Synchronization required

Common synchronization methods:

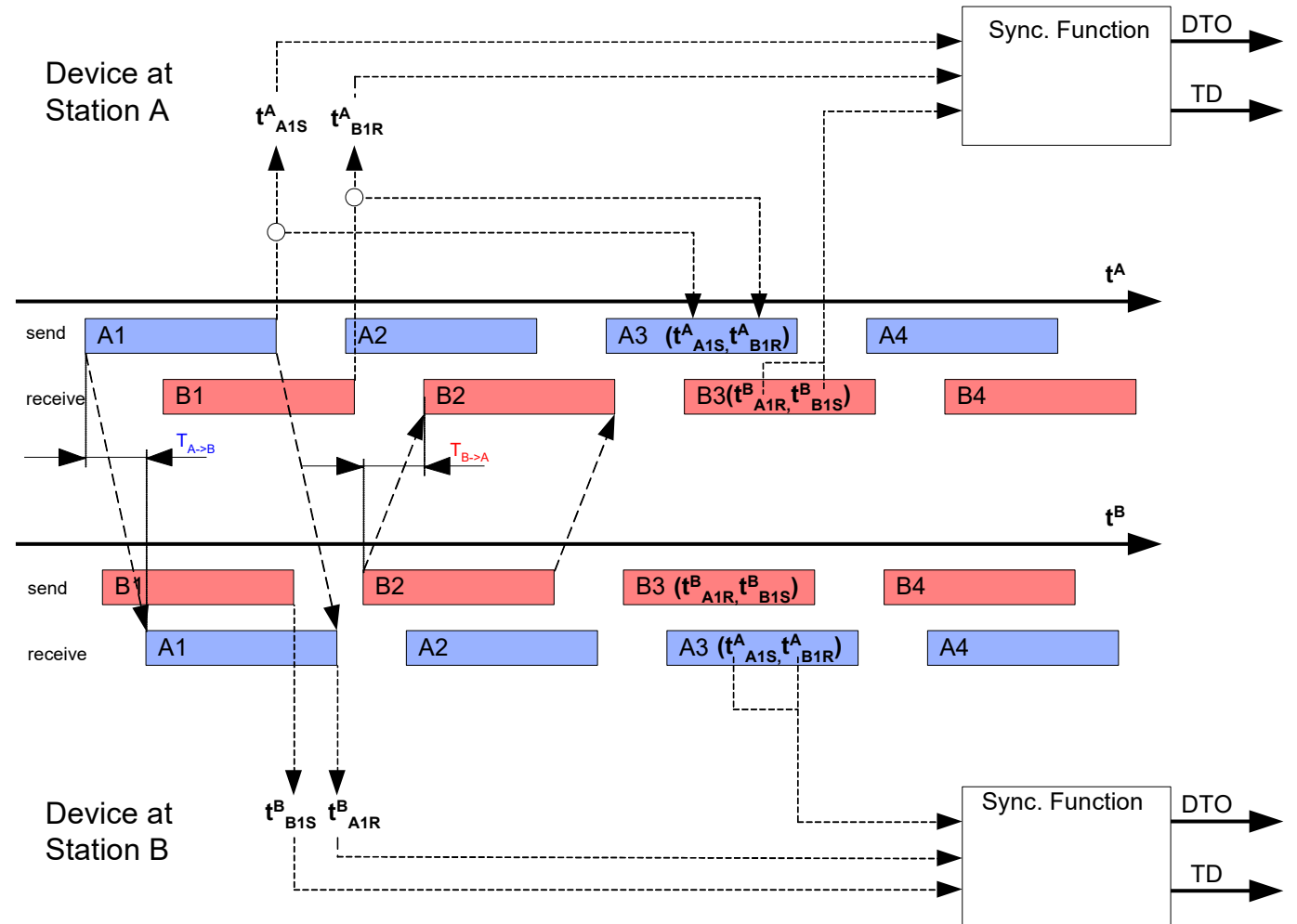
- Ping-pong method
 - Small bandwidth (min. 64 kBit/s)
- Sync. with global time reference
 - \rightarrow PTP, 1PPS, GNSS



7SD8 Line Differential Protection

General – PingPong Method

- Timebase counters running independent in both relays (based on CPU crystal)
 - Device time offset → DTO
 - Transmission delay → TD
 - Timestamps taken with last bit of send/received telegrams
 - Received messages contain remote timestamps
- Estimation of transmission delay
 → Estimation of DTO and DTO drift
 → Microsecond accuracy achieved !



7SD8 Line differential protection

General – Channel delay and DTO supervision

- Transmission delay (TD)
 - Calculated by time difference between send and received telegrams
 - Jumps in transmission delay may occur due to (symmetrical) channel switching
 - Up to 155 ms transmission delays can be tolerated by Line Differential (theory)

- Device time offset (DTO)

- Difference of local and remote time base counter
- No jumps are expected in DTO measurements
 - any DTO jump is assumed as channel asymmetry

$$DTO = TB_{local} - TB_{remote}$$

- Setting for max. tolerated channel asymmetry ΔT_{asym} → restraining current component

SIPROTEC 5

Line Differential Protection

Stabilization Methods

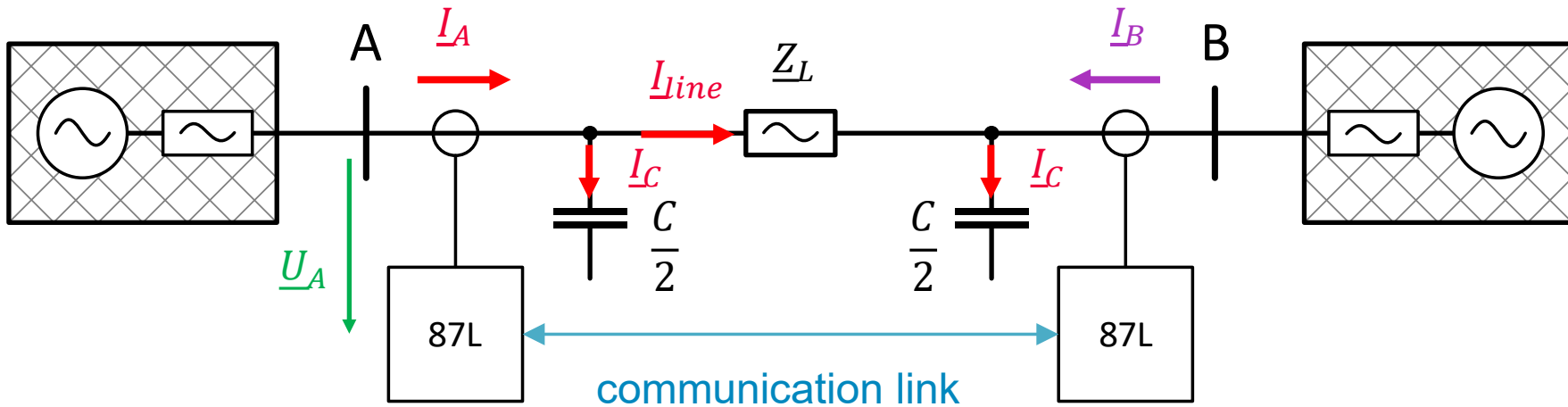
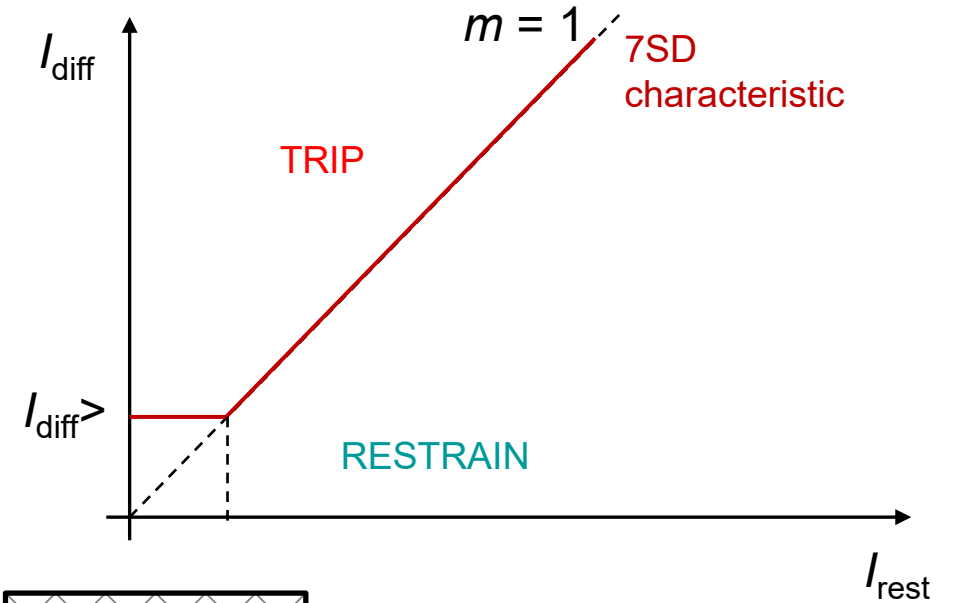
7SD8 Line Differential Protection

Adaptive Restrained Differential Characteristic

- Single slope characteristic

$$I_{diff,ph} = |I_{A,ph} + I_{B,ph}|$$

$$I_{rest,ph} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$



7SD8 Line Differential Protection

Adaptive Restrained Differential Characteristic

- Differential current

$$I_{diff,ph} = |I_{A,ph} + I_{B,ph}|$$

- Restraining current calculated from sum over line ends of max. phase current CT errors and signal distortion:

$$I_{rest,ph} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$

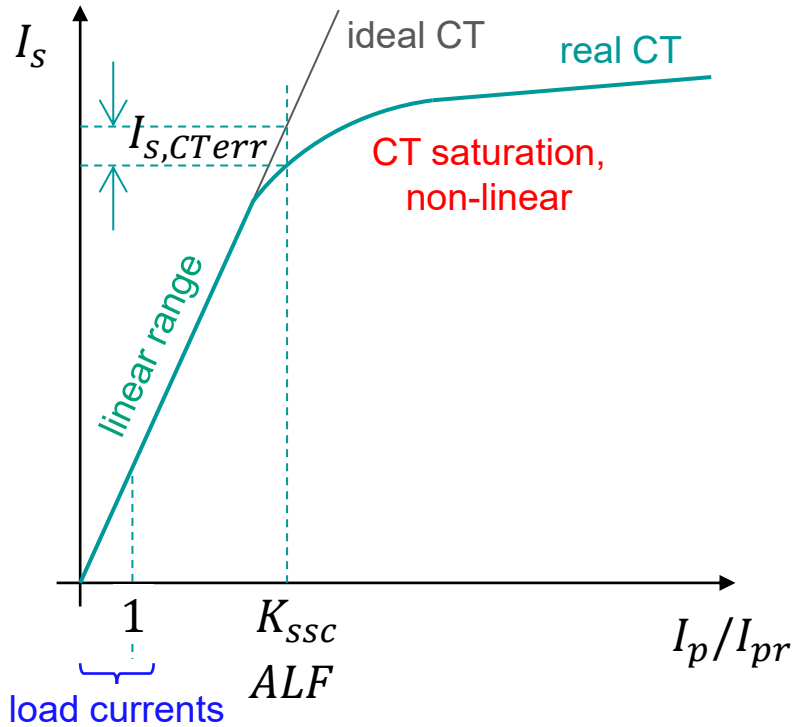
Threshold
parameter

Adaptive stabilization

7SD8 Line Differential Protection

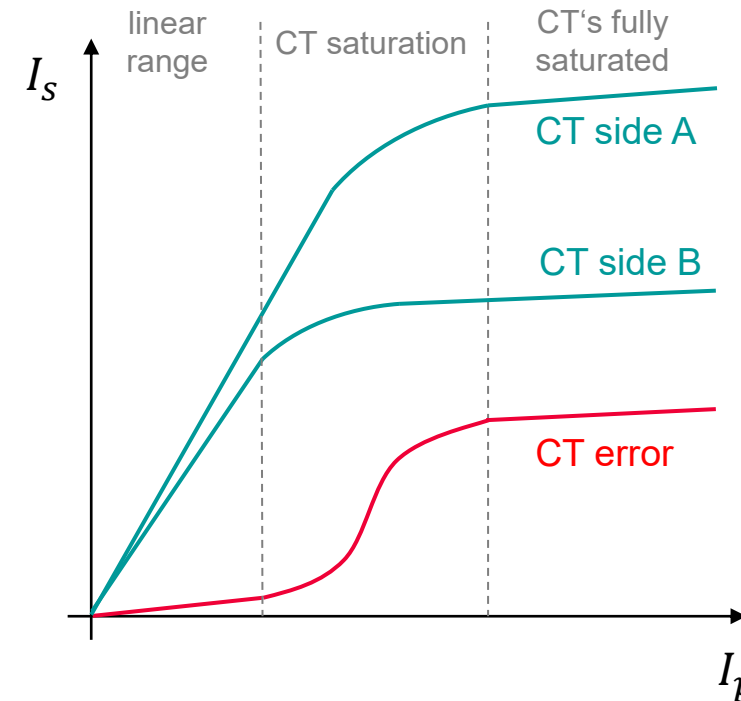
Restraining Current: CT Errors (1)

- Steady state error (e.g. 5P10 → 5% error @ 10 In and R_{br})



$$I_{rest} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$

- Differential current due to CT errors for two line ends

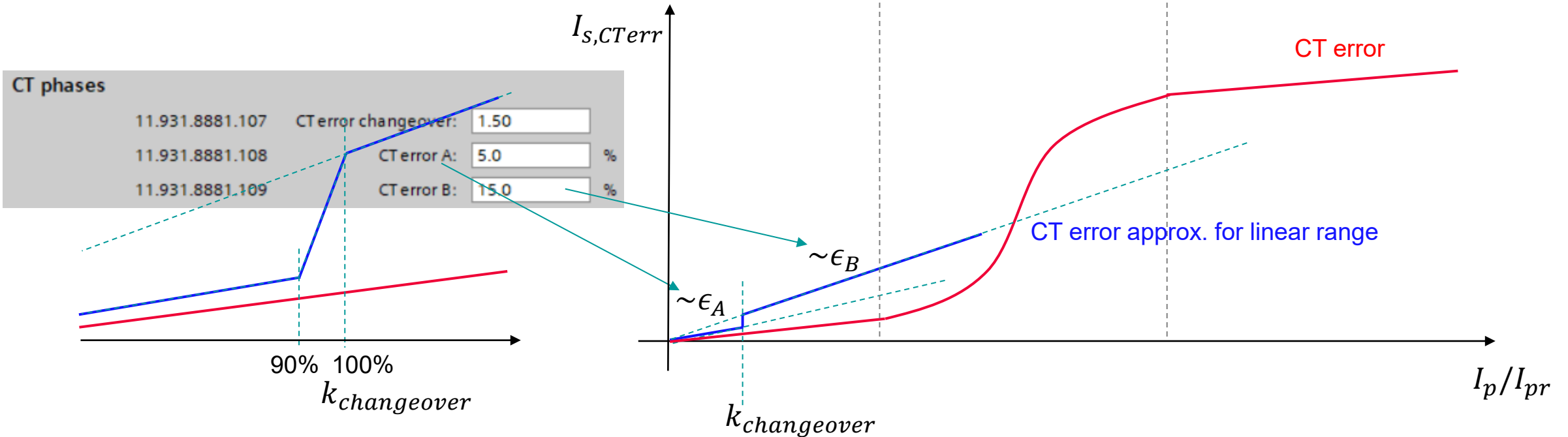


7SD8 Line Differential Protection

Restraining Current: CT Errors (2)

$$I_{rest} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$

- Restraining current component for CT errors in linear range
 - Differential currents due to CT errors are considered (not for CT saturation effects → see next slide)
 - Two slope characteristic
 - Higher sensitivity under load conditions
 - Higher restraining for fault currents



7SD8 Line Differential Protection

Restraining Current: CT Errors (3)

$$I_{rest} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$

- Recommended settings for different CT classes
 - SIP 5 ↔ SIP 5

CT phases

11.931.8881.101	Rated primary current:	<input type="text" value="2400.0"/>	A
11.931.8881.102	Rated secondary current:	<input type="text" value="1 A"/>	
11.931.8881.117	Current range:	<input type="text" value="100 x IR"/>	
11.931.8881.118	Internal CT type:	<input type="text" value="CT protection"/>	
11.931.8881.116	Neutr.point in dir.of ref.obj:	<input type="text" value="yes"/>	
11.931.8881.114	Inverted phases:	<input type="text" value="none"/>	
11.931.8881.107	CTerror changeover:	<input type="text" value="1.50"/>	
11.931.8881.108	CTerror A:	<input type="text" value="3.0"/>	%
11.931.8881.109	CTerror B:	<input type="text" value="10.0"/>	%

Transformer Class	Standard	Ratio Error at Rated Current	Angle Error at Rated Current	Error at Rated Overcurrent Factor	Error Transition ³⁴	CT error A ³⁴	CT error B ³⁴
5P	IEC 60044-1	1.0 %	± 60 min	≤ 5 %	1.50	3.0 %	10.0 %
10P		3.0 %	—	≤ 10 %	1.50	5.0 %	15.0 %
TPX		0.5 %	± 30 min	ε ≤ 10 %	1.50	1.0 %	15.0 %
TPY		1.0 %	± 30 min	ε ≤ 10 %	1.50	3.0 %	15.0 %
TPZ		1.0 %	180 min ± 18 min	ε ≤ 10 % (only I ≈)	1.50	6.0 %	20.0 %
PX	IEC 60044-1 BS: Class X				1.50	3.0 %	10.0 %
C100 to C800	ANSI				1.50	5.0 %	15.0 %
5TPE	IEC 61869-10	1.0 %	± 60 min	≤ 5 %	1.50	5.0 %	15.0 %

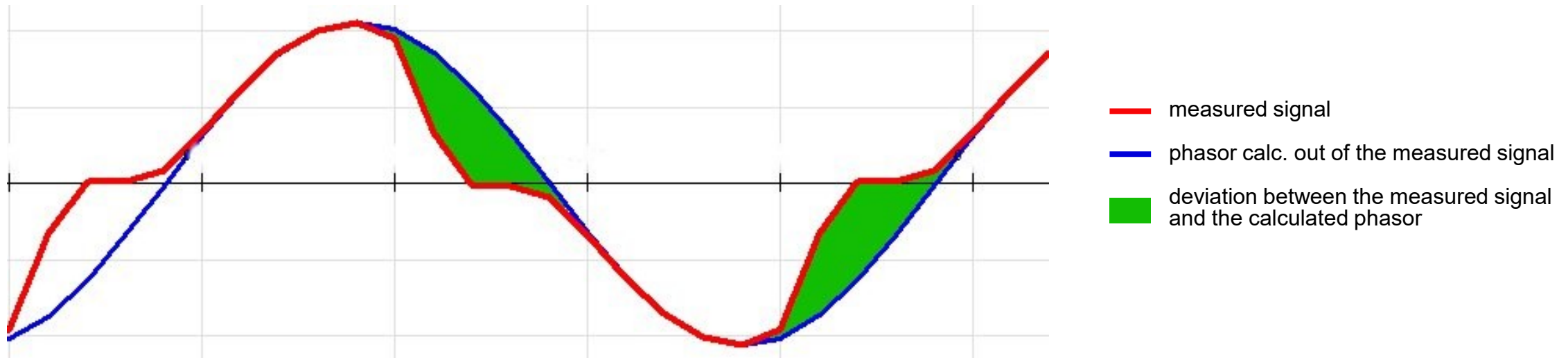
7SD8 Line Differential Protection Restraining Current: Signal Distortion

$$I_{rest} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$

- Differential currents due to CT saturation and signal distortion (e.g. current harmonics)
 - Transient errors

→ Deviation of measured signal compared to fundamental frequency component

→ Adaptive stabilization



7SD8 Line differential protection

Restraining current: Synchronization

$$I_{rest} = I_{thr} + \sum_n I_{ph,CTerr} + \sum_n I_{ph,SigDist} + I_{sync}$$

- Differential currents due to synchronization mismatch
 - Stabilization for asymmetrical transmission delays (difference in Rx and Tx channel)
 - Applications using switched telecommunication networks (SDH, MPLS)

• Example for channel asymmetry

- $T_{A \rightarrow B} = 4 \text{ ms}$
- $T_{B \rightarrow A} = 3 \text{ ms}$

} $TD = 3.5 \text{ ms}$

Estimated by both relays

} $\Delta TD = \pm 0.5 \text{ ms}$

} $\Delta \varphi = \pm 9^\circ @ 50 \text{ Hz}$

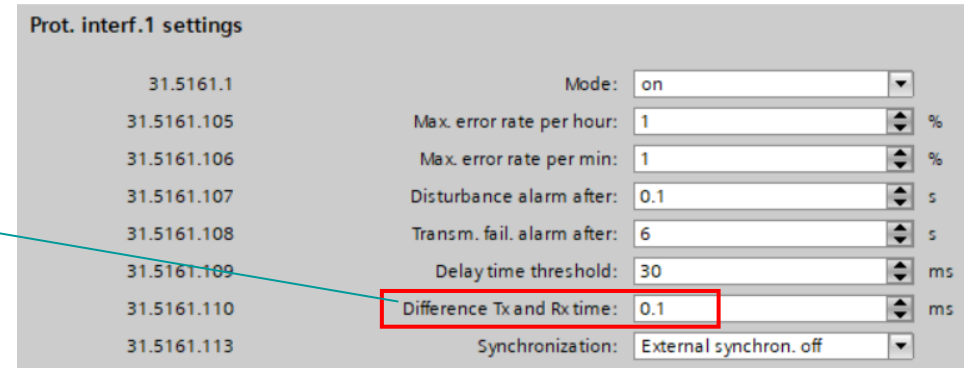
Synchronization error

} $I_{diff} \approx I_{load} \cdot |1 - e^{j \Delta \varphi}|$

Apparent differential current

- Ask your comms-experts for expected channel asymmetry
- Set the max. expected difference in Tx and Rx asymmetry

- Direct FO connections → set to **0 ms**
- IEEE C37.94 interfaces → set to **0.3 ms ... 0.6 ms**



SIPROTEC 5

Line Differential Protection Stages

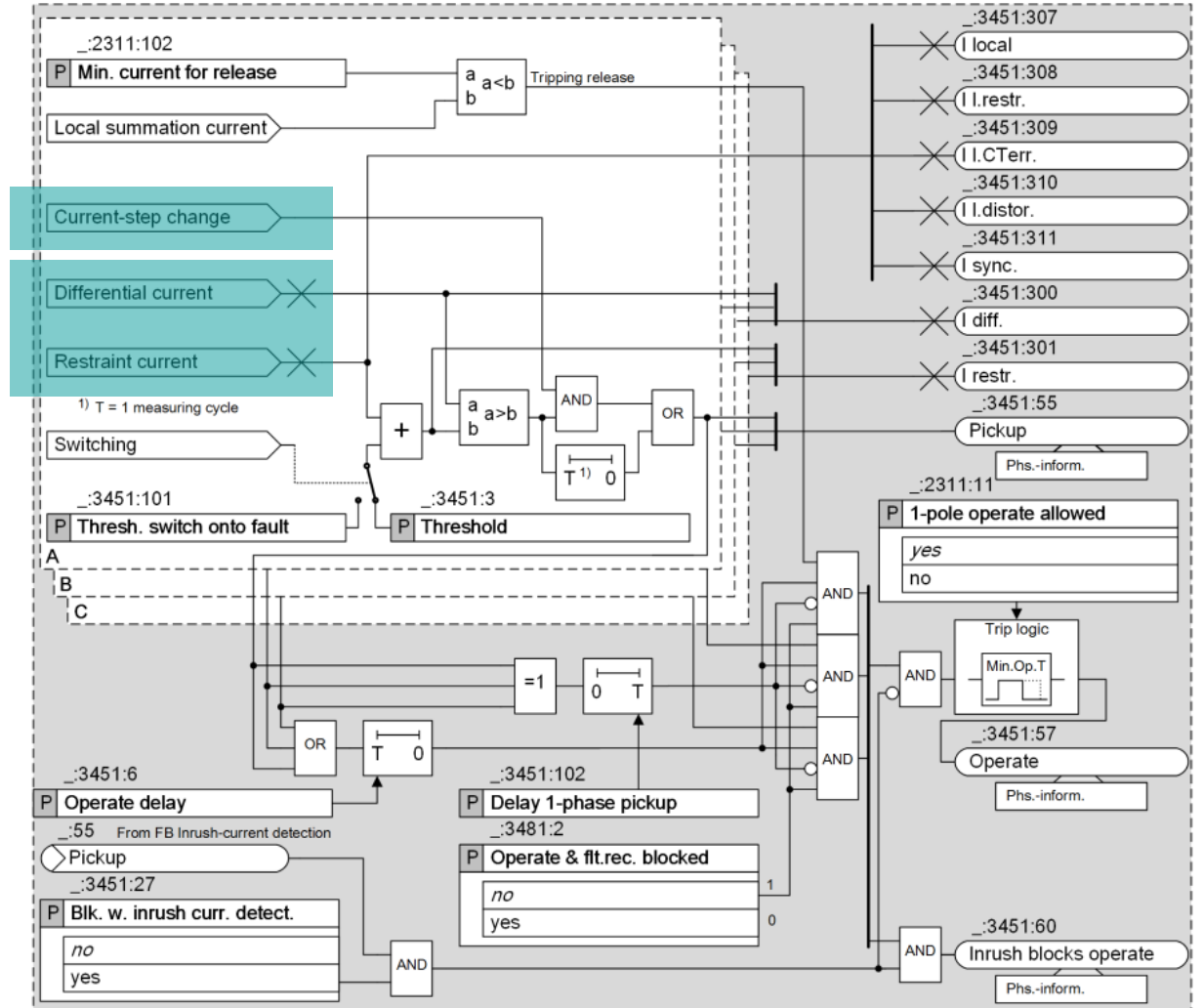
7SD8 Line Differential Protection

“I-DIFF” Stage

- Core protection stage
 - Based on current phasors
 - Two settable thresholds for I-DIFF >
 - Optional Time delay
- Current jump detection to speed up operation

I-DIFF

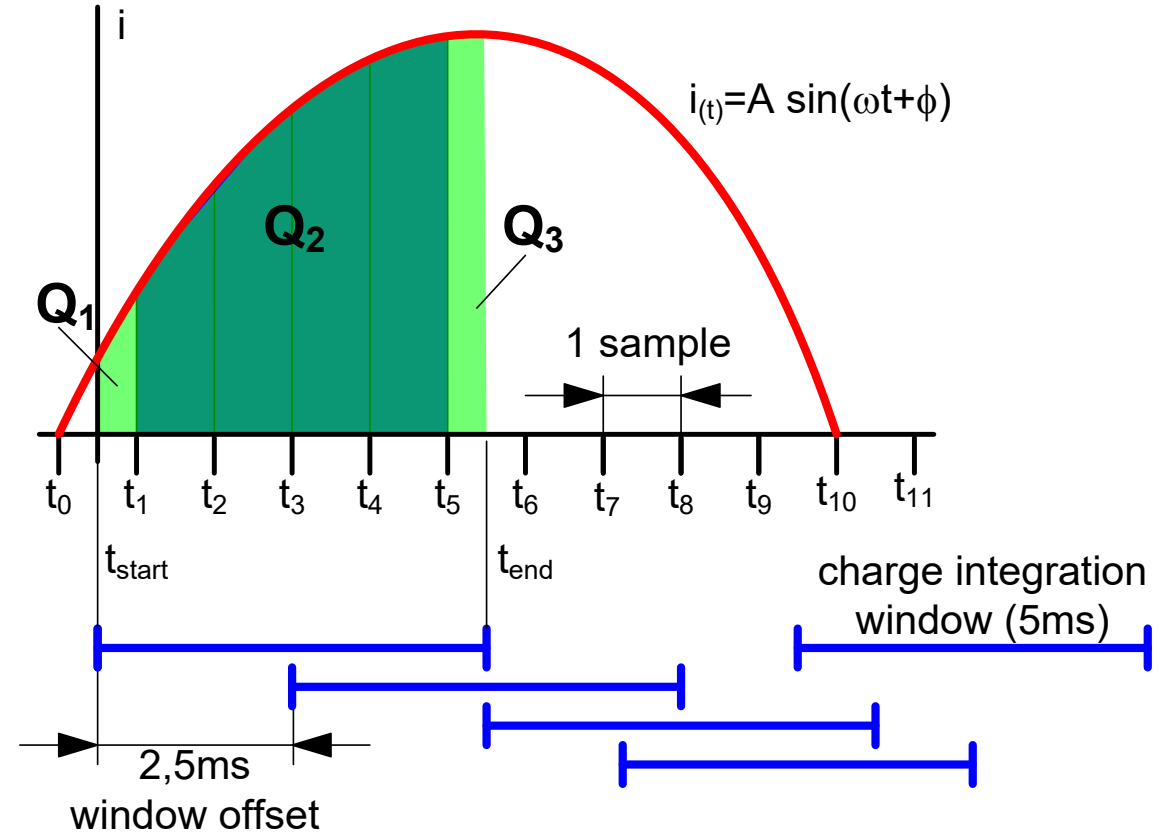
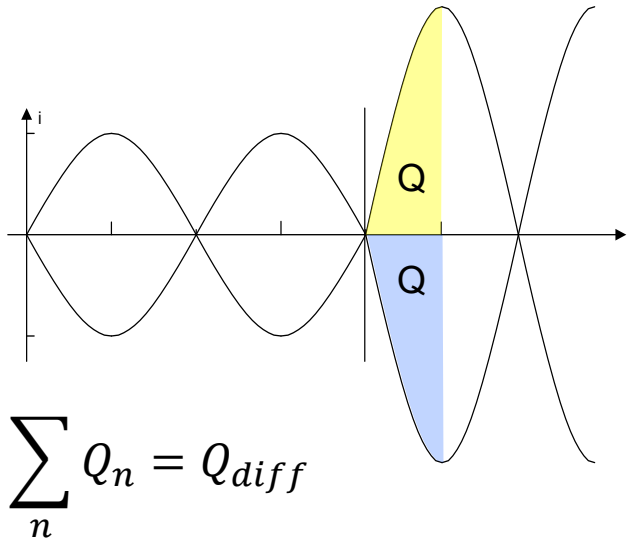
21.831.3451.1	Mode:	<input type="text" value="on"/>	
21.831.3451.2	Operate & ft.rec. blocked:	<input type="text" value="no"/>	
21.831.3451.3	Threshold:	<input type="text" value="0.300"/>	A
21.831.3451.101	Thresh. switch onto fault:	<input type="text" value="0.300"/>	A
21.831.3451.6	Operate delay:	<input type="text" value="0.00"/>	s



7SD8 Line Differential Protection

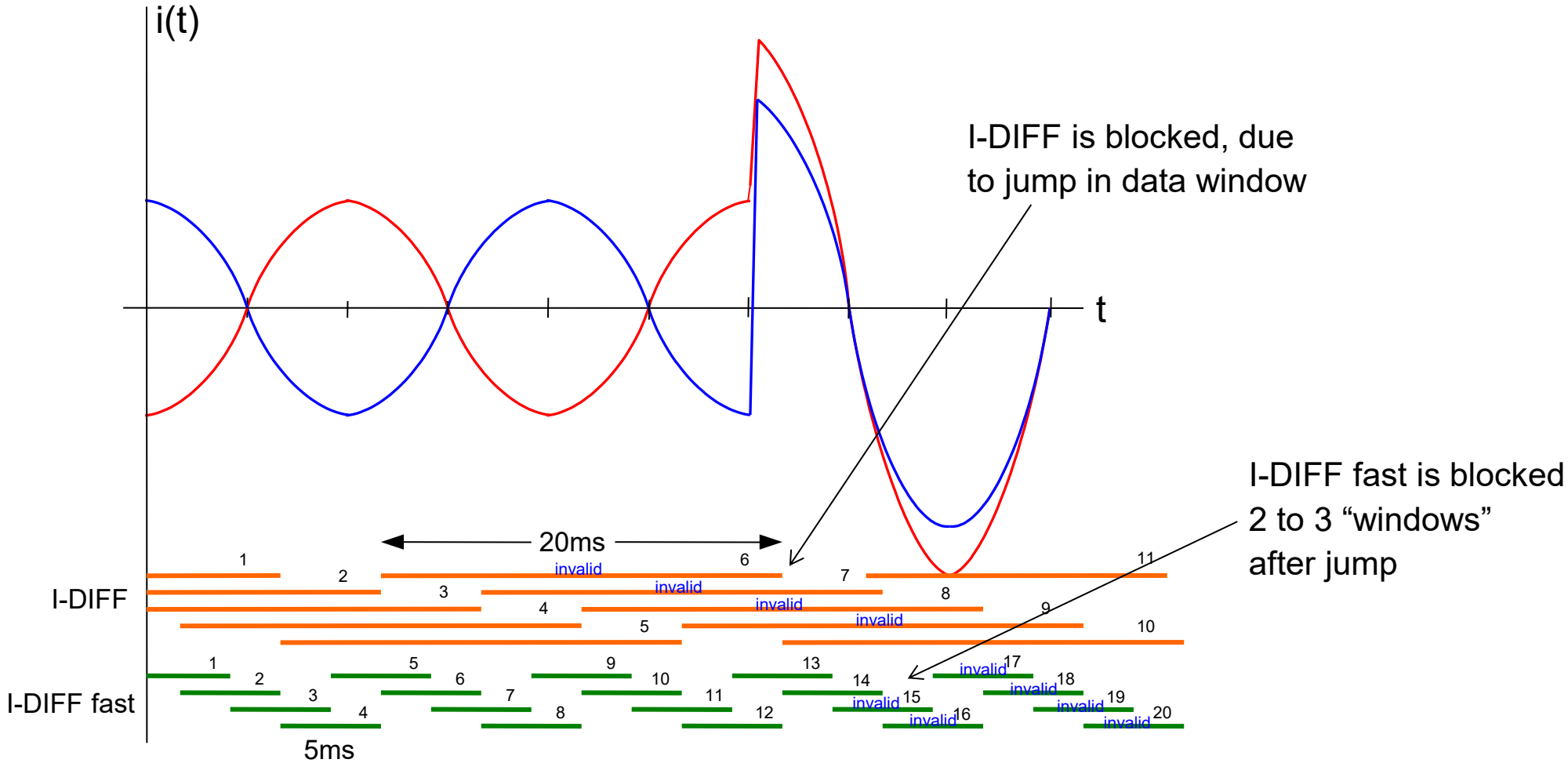
“I-DIFF Fast” and “I-DIFF Fast 2” Stage

- Charge based differential principle
- Charge is calculated from current samples
→ 5 ms data windows
- Stage active only for high currents
→ allows faster tripping than I-DIFF stage
- Differential charge Q_{diff} is calculated at all line ends
- Instantaneous tripping (time delay setting from V9.80)



7SD8 Line Differential Protection

“I-DIFF Fast 2” and “I-DIFF” Stage at Fault Inception

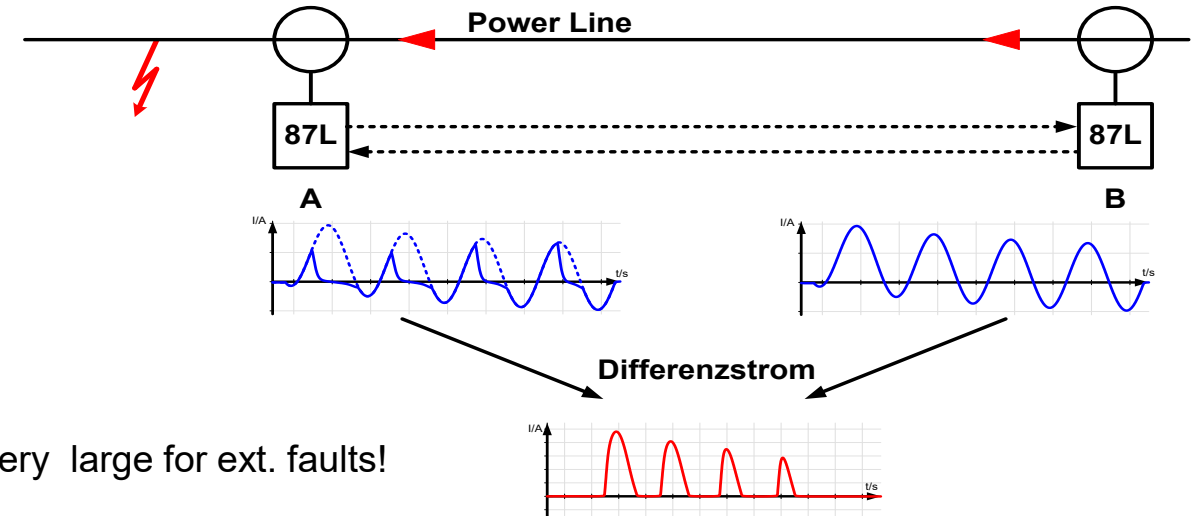


7SD8 Line Differential Protection

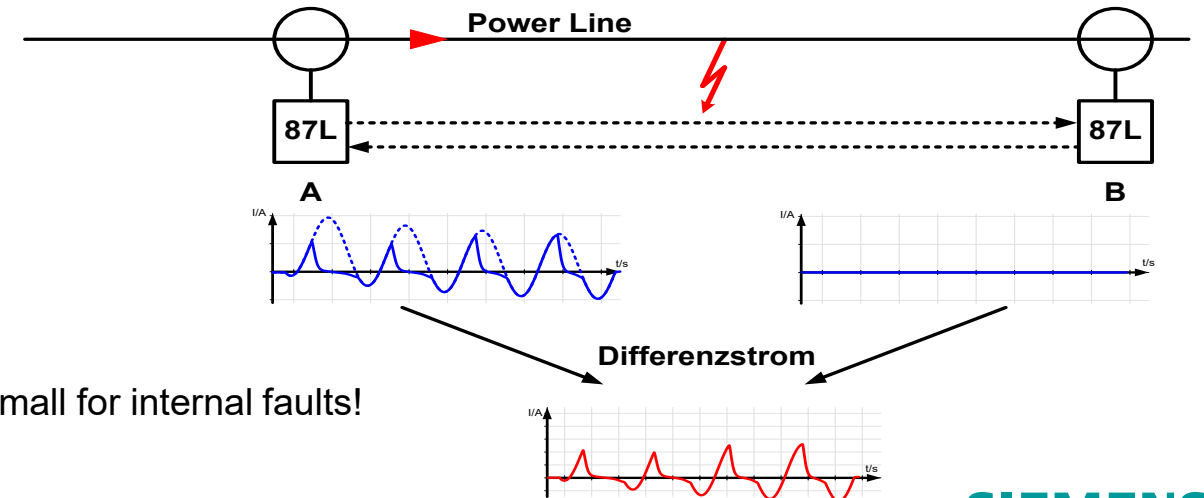
“I-DIFF Fast 2” Stage – New Saturation Detection

Problem:

- CT saturation can result in conditions where the differential current during internal fault is smaller than for external faults!
- High fault currents with saturation can result in blocking of the „I-DIFF fast“ stage
- “I-DIFF fast” stage is not fast enough for all applications...



Could be very large for ext. faults!



Could be small for internal faults!

7SD8 Line Differential Protection

“I-DIFF Fast 2” Stage – New Saturation Detection with Matching “I-DIFF Fast” Stage

Solution:

→ Saturation detection based on waveform analysis!

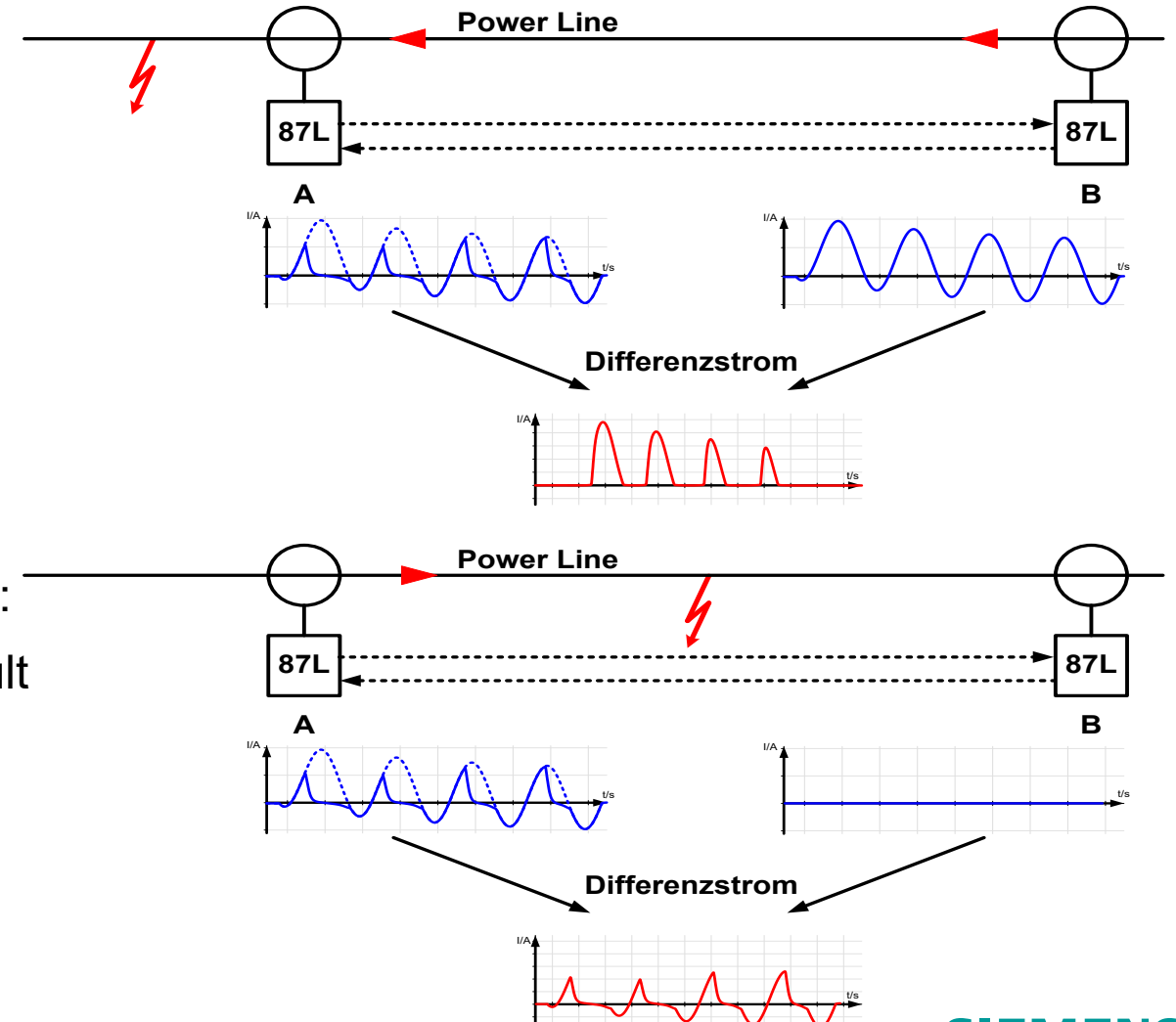
Advantages in SIPROTEC 5:

- I-DIFF stage → No changes
- I-DIFF fast stage → Still available (compatibility to existing SIPROTEC 4 relays)
- I-DIFF fast 2 → New, improved including saturation detector

Response of “I-DIFF fast 2” when saturation is detected:

- Blocked when saturation is detected and external fault
- Not blocked for internal faults
- Fault changes from external to internal are cleared faster

→ Better response for high fault currents

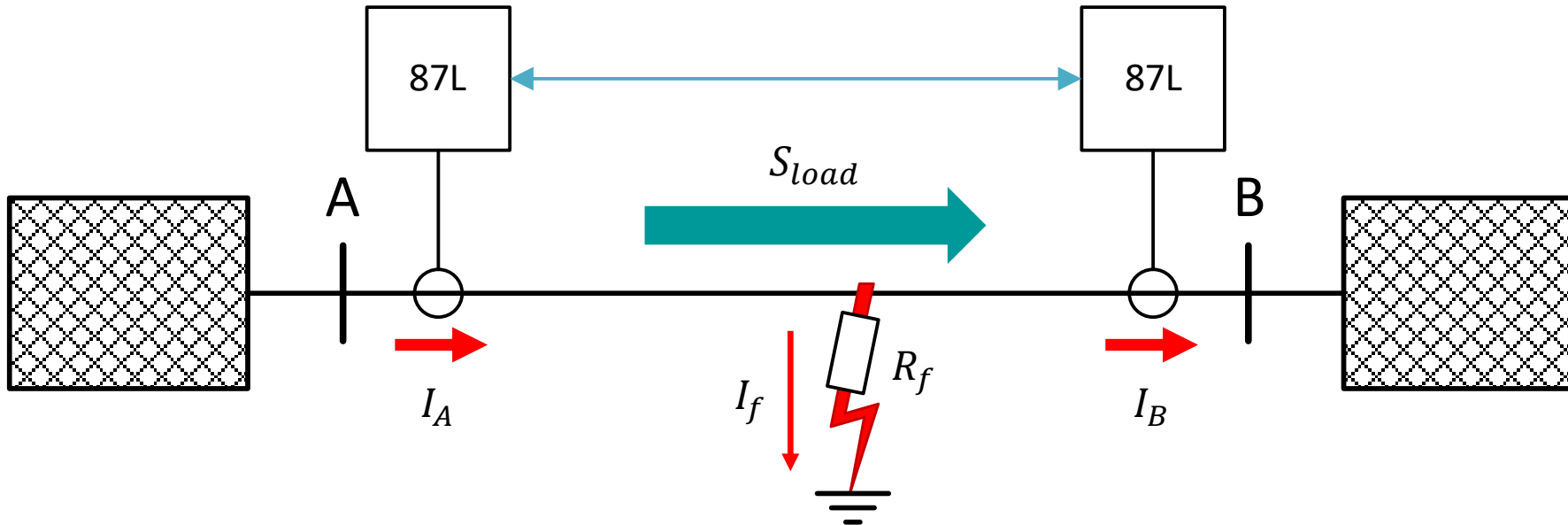


7SD8 Line Differential Protection

Sensitive Earth Fault and Unsymmetrical Stages

(from V09.30)

- High load current at line \rightarrow high restraining currents
- Reduced sensitivity for high impedance faults



\rightarrow Use “IN-DIFF” or “I2-DIFF” Stages for special applications

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